

Features

- 80MHz RISC MCU and 80MIPS Kalimba DSP
- Internal ROM, serial flash memory and EEPROM interfaces
- Stereo codec with 2 microphone inputs
- Radio includes integrated balun
- 5-band fully configurable EQ
- CSR's latest CVC technology for narrowband and wideband voice connections including wind noise reduction
- Wideband speech supported by HFP v1.6 profile and mSBC codec
- Voice recognition support for answering a call, enables true hands-free use
- Multipoint HFP connection to 2 phones for voice
- Multipoint A2DP connection enables a headset (A2DP) connection to 2 A2DP source devices for music playback
- Secure simple pairing, CSR's proximity pairing and CSR's proximity connection
- Audio interfaces: I²S and PCM
- Serial interfaces: UART, USB 2.0 (full-speed), I²C and SPI
- aptX, SBC, MP3 and AAC decoder support
- Wired audio support (USB and analogue)
- Support for smartphone/tablet applications
- Integrated dual switch-mode regulators, linear regulators and battery charger
- External crystal load capacitors not required for typical crystals
- 3 LED outputs
- 68-ball VFBGA 5.5 x 5.5 x 1mm 0.5mm pitch
- Green (RoHS compliant and no antimony or halogenated flame retardants)

General Description

BlueCore® CSR8645™ BGA is a product from CSR's Connectivity Centre. It is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including basic rate, EDR to 3Mbps and Bluetooth low energy.

The integrated peripherals reduce the number of external components required, including no requirement for external codec, battery charger, SMPS, LDOs, balun or external program memory, ensuring minimum production costs.

The battery charger architecture enables the CSR8645 BGA to independently operate from the charger supply, ensuring dependable operation for all battery conditions.

BlueCore® CSR8645™ BGA

CSR8645 Stereo ROM Solution with aptX™

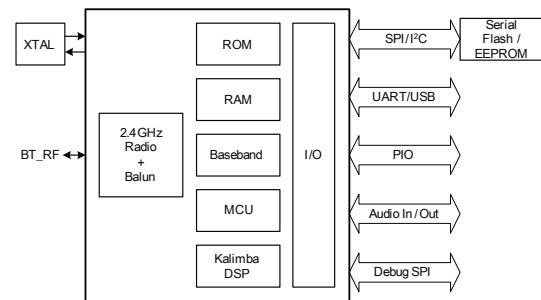
2-mic CVC Audio Enhancement

Fully Qualified Single-chip Bluetooth® v4.0 System

Production Information

CSR8645A04

Issue 6



Applications

- Stereo headsets
- Wired stereo headsets and headphones
- Portable stereo speakers

The enhanced Kalimba DSP coprocessor with 80MIPS supports enhanced audio and DSP applications.

The integrated audio codec supports 2 channels of ADC, 2 digital microphone inputs and stereo output, as well as a variety of audio standards.

See *CSR Glossary* at www.csrsupport.com.

Ordering Information

| Device | Package | | | Order Number |
|---------------------------------------|-------------------------|--------------------------------|-----------------|-------------------|
| | Type | Size | Shipment Method | |
| CSR8645 Stereo ROM Solution with aptX | VFBGA-68-ball (Pb free) | 5.5 x 5.5 x 1mm 0.5mm pitch | Tape and reel | CSR8645A04-IBBC-R |

Note:

CSR8645 BGA is a ROM-based device where the product code has the form CSR8645Axx. Axx is the specific ROM-variant, A04 is the ROM-variant for CSR8645 Stereo ROM Solution with aptX.

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

Contacts

| | |
|-------------------------------------|--|
| General information | www.csr.com |
| Information on this product | Sales@csr.com |
| Customer support for this product | www.crsupport.com |
| Details of compliance and standards | Product.compliance@csr.com |
| Help with this document | Comments@csr.com |

CSR8645 Stereo ROM Solution with aptX Development Kit Ordering Information

| Description | Order Number |
|---|------------------|
| CSR8645 Stereo ROM Solution with aptX Audio Development Kit | DK-8645-10064-1A |

Device Details

Bluetooth low energy

- Dual-mode Bluetooth low energy radio
- Support for Bluetooth basic rate / EDR and low energy connections
- 3 Bluetooth low energy connections at the same time as basic rate A2DP

Bluetooth Radio

- On-chip balun (50Ω impedance)
- No production trimming of external components
- Bluetooth v4.0 specification compliant

Bluetooth Transmitter

- 9dBm (typical) RF transmit power with level control
- Class 1, Class 2 and Class 3 support, no external PA or TX/RX switch required

Bluetooth Receiver

- -92dBm (typical) π/4 DQPSK receiver sensitivity and -82dBm (typical) 8DPSK receiver sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available to application
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Bluetooth Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 32MHz

Kalimba DSP

- Enhanced Kalimba DSP coprocessor, 80MIPS, 24-bit fixed point core
- 2 single-cycle MACs; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 6K x 32-bit program RAM including 1K instruction cache for executing out of internal ROM
- 16K x 24-bit + 16K x 24-bit 2-bank data RAM

Audio Interfaces

- Audio codec with 2 high-quality dedicated ADCs
- Microphone bias generator and up to 2 analogue microphone inputs
- 2 digital microphone inputs (MEMS)
- Enhanced side-tone gain control
- Supported sample rates of 8, 11.025, 16, 22.05, 32, 44.1, 48 and 96kHz (DAC only)

Auxiliary Features

- Crystal oscillator with built-in digital trimming

Package Option

- 68-ball VFBGA 5.5 x 5.5 x 1mm 0.5mm pitch

Physical Interfaces

- UART interface for debug
- USB 2.0 (full-speed) interface for audio and charger enumeration
- 1-bit SPI flash memory interface
- SPI interface for debug and programming
- I²C interface for EEPROM
- Up to 22 general purpose PIOs with 3 extra open-drain PIOs available when LED not used
- PCM and I²S interfaces
- 3 LED drivers (includes RGB) with PWM flasher independent of MCU

Integrated Power Control and Regulation

- Automatic power switching to charger when present
- 2 high-efficiency switch-mode regulators with 1.8V and 1.35V outputs direct from battery supply
- 3.3V linear regulator for USB supply
- Low-voltage linear regulator for internal digital circuits
- Low-voltage linear regulator for internal analogue circuits
- Power-on-reset detects low supply voltage
- Power management includes digital shutdown and wake-up commands for ultra-low power modes

Battery Charger

- Lithium ion / Lithium polymer battery charger
- Instant-on function automatically selects the power supply between battery and USB, which enables operation even if the battery is fully discharged
- Fast charging support up to 200mA with no external components
- Higher charge currents using external pass device
- Supports USB charger detection
- Support for thermistor protection of battery pack
- Support to enable end product design to PSE law:
 - Design to JIS-C 8712/8714 (batteries)
 - Testing based on IEEE 1725

Baseband and Software

- Internal ROM
- Memory protection unit supporting accelerated VM
- 56KB internal RAM, enables full-speed data transfer, mixed voice/data and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

CSR8645 Stereo ROM Solution with aptX Details

Bluetooth Profiles

- Bluetooth v4.0 specification support
- HFP v1.6 wideband speech (HD voice ready)
- HSP v1.2
- A2DP v1.2
- AVRCP v1.4
- Support for smartphone applications (apps)

Improved Audio Quality

CSR's latest 2-mic CVC audio enhancements for narrowband and wideband connections including:

- 2-mic far-end audio enhancements
- Near-end audio enhancements (noise suppression and AEQ)
- Wind noise reduction
- Packet loss concealment
- Bit error concealment
- Automatic gain control and automatic volume control
- Frequency expansion for improved speech intelligibility
- mSBC codec support for wideband speech

Music Enhancements

- Configurable 5-band EQ for music playback (rock, pop, classical, jazz, dance etc)
- aptX, SBC, MP3, AAC and Faststream decoder
- Stereo widening (S3D)
- Volume Boost

Additional Functionality

- Support for voice recognition
- Support for multi-language programmable audio prompts
- CSR's proximity pairing and CSR's proximity connection
- Multipoint support for HFP connection to 2 handsets for voice
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Talk-time extension

CSR8600 ROM Series Configuration Tool

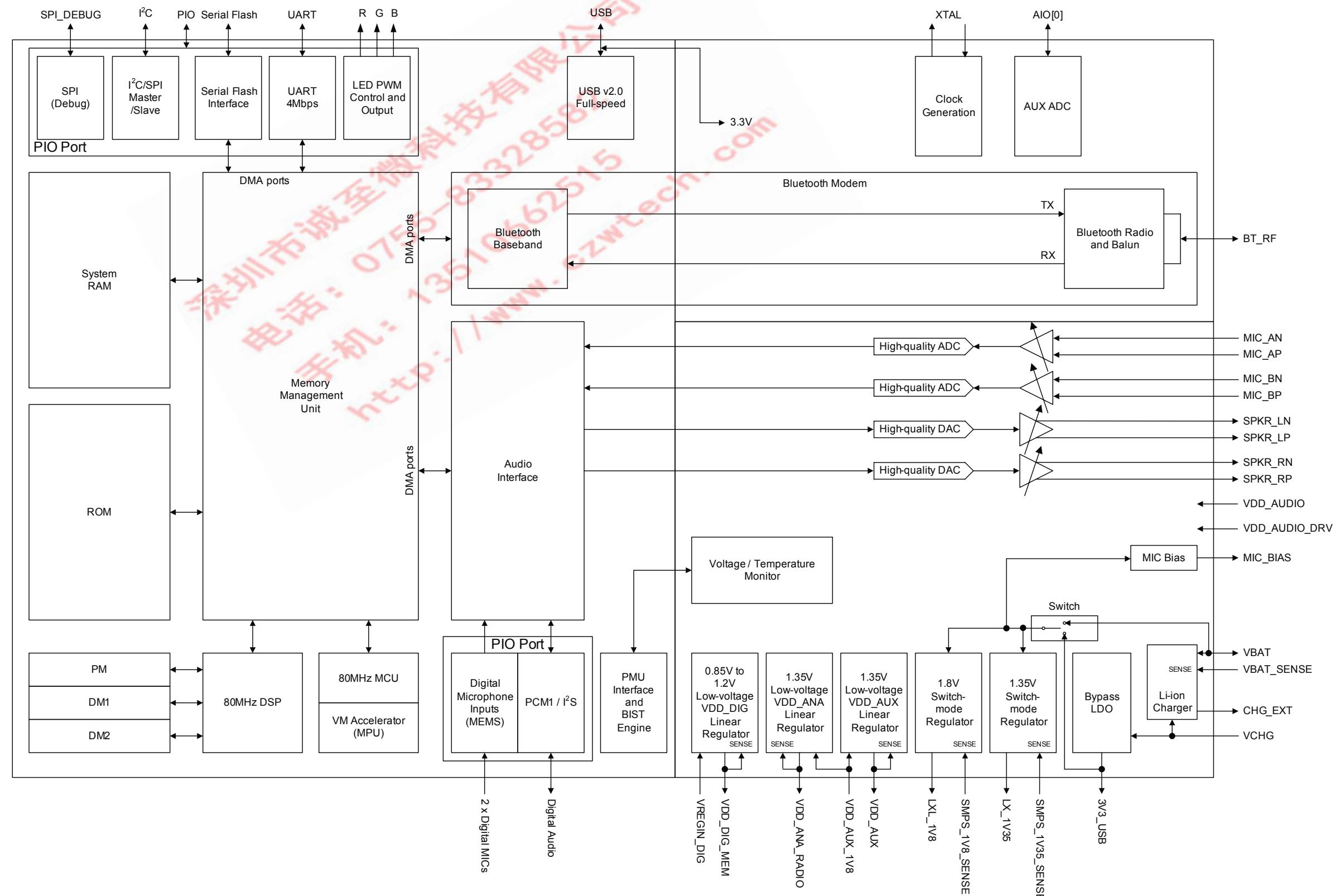
Configures the CSR8645 stereo ROM solution with aptX software features:

- Bluetooth v4.0 specification features
- Reconnection policies, e.g. reconnect on power-on
- Audio features, including default volumes
- Button events: configuring button presses and durations for certain events, e.g. double press on PIO for last number redial
- LED indications for states, e.g. headset connected, and events, power on etc.
- Indication tones for events and ringtones
- HFP v1.6 supported features
- Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
- Advanced Multipoint settings

CSR8645 Stereo ROM Solution with aptX Development Kit

- CSR8645 stereo ROM solution with aptX demonstrator board (DB-8645-10067-1A)
- Interface adapters and cables are available
- Works in conjunction with the CSR8600 ROM Series Configuration Tool and other supporting utilities

Functional Block Diagram



Document History

| Revision | Date | Change Reason |
|----------|-----------|--|
| 1 | 24 AUG 11 | Internal publication of this document. |
| 2 | 13 SEP 11 | Original publication of this document. |
| 3 | 28 SEP 11 | Editorial updates. |
| 4 | 17 JAN 12 | Bluetooth v4.0 specification added. Pre-production status. Power consumption figures added. Package Dimensions updated and pin configuration drawing removed. Editorial updates. |
| 5 | 02 FEB 12 | Internal release. |
| 6 | 06 FEB 12 | Production Information added. If you have any comments about this document, email comments@csr.com giving number, title and section with your feedback. |

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-critical Applications

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CSR Green Semiconductor Products and RoHS Compliance

CSR8645 BGA devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

CSR8645 BGA devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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Refer to www.csrsupport.com for compliance and conformance to standards information.

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1 Package Information

1.1 Pinout Diagram

Orientation from Top of Device

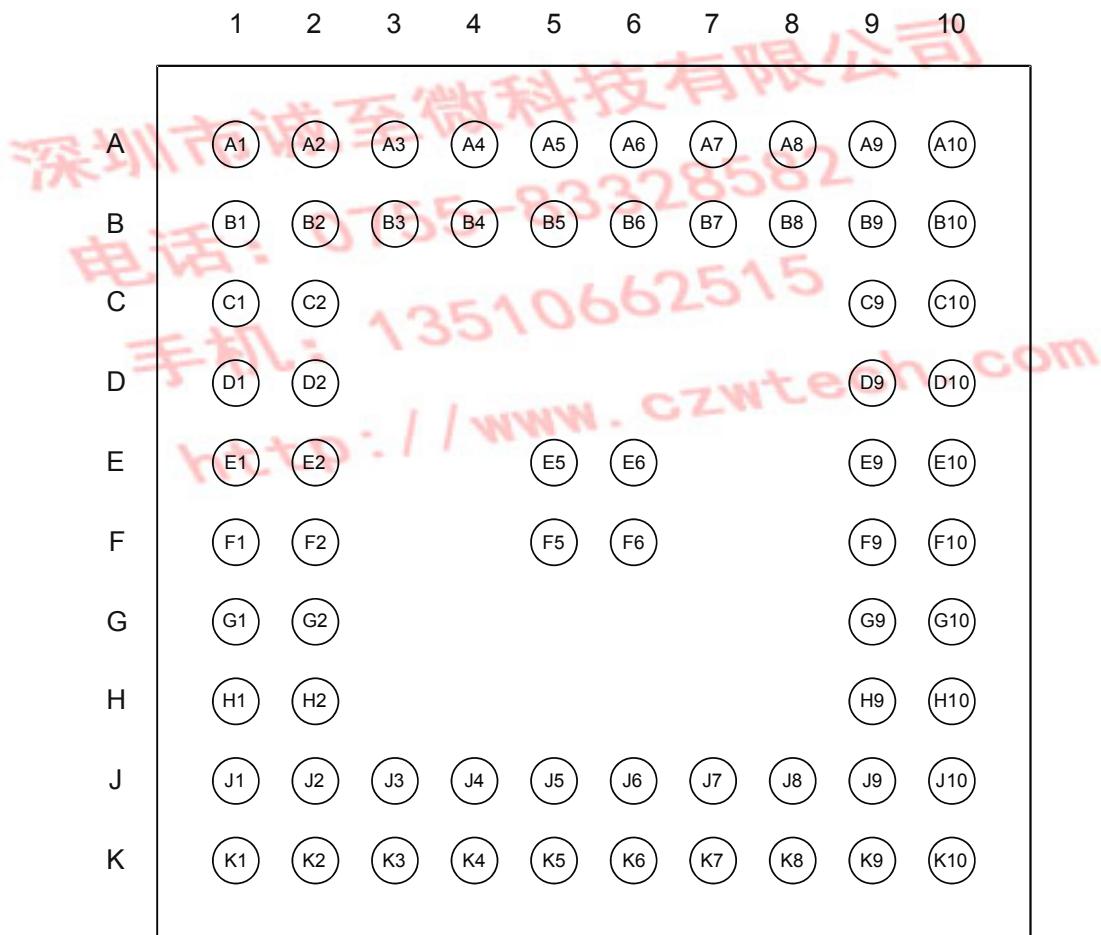


Figure 1.1: Device Pinout

G-TW-0007438-1.1

1.2 Device Terminal Functions

| Radio | Ball | Pad Type | Supply Domain | Description |
|-------|------|----------|---------------|---|
| BT_RF | A3 | RF | VDD_ANA_RADIO | Bluetooth 50Ω transmitter output / receiver input |

| Oscillator | Ball | Pad Type | Supply Domain | Description |
|------------|------|----------|---------------|-------------------------------------|
| XTAL_IN | C1 | | | For crystal or external clock input |
| XTAL_OUT | B1 | Analogue | VDD_AUX | Drive for crystal |

| USB | Ball | Pad Type | Supply Domain | Description |
|-------|------|---------------|---------------|---|
| USB_P | H10 | Bidirectional | 3V3_USB | USB data plus with selectable internal 1.5kΩ pull-up resistor |
| USB_N | J10 | | | USB data minus |

| SPI/PCM Interface | Ball | Pad Type | Supply Domain | Description |
|-------------------|------|---------------------------|---------------|--|
| SPI_PCM# | J4 | Input with weak pull-down | VDD_PADS_1 | SPI/PCM# select input: <ul style="list-style-type: none">■ 0 = PCM/PIO interface■ 1 = SPI |

Note:

SPI and PCM1 interfaces are mapped as alternative functions on the PIO port.

| PIO Port | Ball | Pad Type | Supply Domain | Description |
|----------|------|-------------------------------------|---------------|--|
| PIO[21] | D10 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable input / output line 21. |
| PIO[20] | C10 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable input / output line 20. |
| PIO[19] | C9 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable input / output line 19. |
| PIO[18] | D9 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable input / output line 18. |
| PIO[17] | H2 | Bidirectional with strong pull-down | VDD_PADS_1 | Programmable input / output line 17. Alternative function: <ul style="list-style-type: none">■ UART_CTS: UART clear to send, active low |

| PIO Port | Ball | Pad Type | Supply Domain | Description |
|----------|------|-------------------------------------|---------------|--|
| PIO[16] | F1 | Bidirectional with strong pull-up | VDD_PADS_1 | Programmable input / output line 16. Alternative function: <ul style="list-style-type: none">■ UART_RTS: UART request to send, active low |
| PIO[15] | D1 | Bidirectional with strong pull-up | VDD_PADS_1 | Programmable input / output line 15. Alternative function: <ul style="list-style-type: none">■ UART_TX: UART data output |
| PIO[14] | F2 | Bidirectional with strong pull-up | VDD_PADS_1 | Programmable input / output line 14. Alternative function: <ul style="list-style-type: none">■ UART_RX: UART data input |
| PIO[13] | G1 | Bidirectional with strong pull-down | VDD_PADS_1 | Programmable input / output line 13. Alternative function: <ul style="list-style-type: none">■ QSPI_IO[1]: SPI flash data bit 1 |
| PIO[12] | E2 | Bidirectional with strong pull-up | VDD_PADS_1 | Programmable input / output line 12. Alternative function: <ul style="list-style-type: none">■ QSPI_FLASH_CS#: SPI flash chip select■ I2C_WP: I²C bus memory write protect line |
| PIO[11] | G2 | Bidirectional with strong pull-down | VDD_PADS_1 | Programmable input / output line 11. Alternative function: <ul style="list-style-type: none">■ QSPI_IO[0]: SPI flash data bit 0■ I2C_SDA: I²C serial data line |
| PIO[10] | F5 | Bidirectional with strong pull-down | VDD_PADS_1 | Programmable input / output line 10. Alternative function: <ul style="list-style-type: none">■ QSPI_FLASH_CLK: SPI flash clock■ I2C_SCL: I²C serial clock line |
| PIO[9] | G9 | Bidirectional with strong pull-down | VDD_PADS_2 | Programmable input / output line 9. Alternative function: <ul style="list-style-type: none">■ UART_CTS: UART clear to send, active low |
| PIO[8] | E10 | Bidirectional with strong pull-up | VDD_PADS_2 | Programmable input / output line 8. Alternative function: <ul style="list-style-type: none">■ UART_RTS: UART request to send, active low |
| PIO[7] | G10 | Bidirectional with strong pull-down | VDD_PADS_2 | Programmable input / output line 7. |
| PIO[6] | E9 | Bidirectional with strong pull-down | VDD_PADS_2 | Programmable input / output line 6. |

| PIO Port | Ball | Pad Type | Supply Domain | Description |
|----------|------|-----------------------------------|---------------|---|
| PIO[5] | J1 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable input / output line 5. Alternative function: <ul style="list-style-type: none">■ SPI_CLK: SPI clock■ PCM1_CLK: PCM1 synchronous data clock |
| PIO[4] | E1 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable input / output line 4. Alternative function: <ul style="list-style-type: none">■ SPI_CS#: chip select for SPI, active low■ PCM1_SYNC: PCM1 synchronous data sync |
| PIO[3] | J5 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable input / output line 3. Alternative function: <ul style="list-style-type: none">■ SPI_MISO: SPI data output■ PCM1_OUT: PCM1 synchronous data output |
| PIO[2] | H1 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable input / output line 2. Alternative function: <ul style="list-style-type: none">■ SPI_MOSI: SPI data input■ PCM1_IN: PCM1 synchronous data input |
| PIO[1] | F10 | Bidirectional with strong pull-up | VDD_PADS_2 | Programmable input / output line 1. Alternative function: <ul style="list-style-type: none">■ UART_TX: UART data output |
| PIO[0] | F9 | Bidirectional with strong pull-up | VDD_PADS_2 | Programmable input / output line 0. Alternative function: <ul style="list-style-type: none">■ UART_RX: UART data input |
| AIO[0] | D2 | Bidirectional | VDD_AUX | Analogue programmable input / output line 0. |

| Test and Debug | Ball | Pad Type | Supply Domain | Description |
|----------------|------|---------------------------|---------------|--|
| RST# | J3 | Input with strong pull-up | VDD_PADS_1 | Reset if low. Pull low for minimum 5ms to cause a reset. |

| Codec | Ball | Pad Type | Supply Domain | Description |
|--------|------|-------------|---------------|--------------------------------------|
| MIC_AP | A9 | Analogue in | VDD_AUDIO | Microphone input positive, channel A |
| MIC_AN | A10 | | | Microphone input negative, channel A |
| MIC_BP | B7 | Analogue in | VDD_AUDIO | Microphone input positive, channel B |
| MIC_BN | B8 | | | Microphone input negative, channel B |

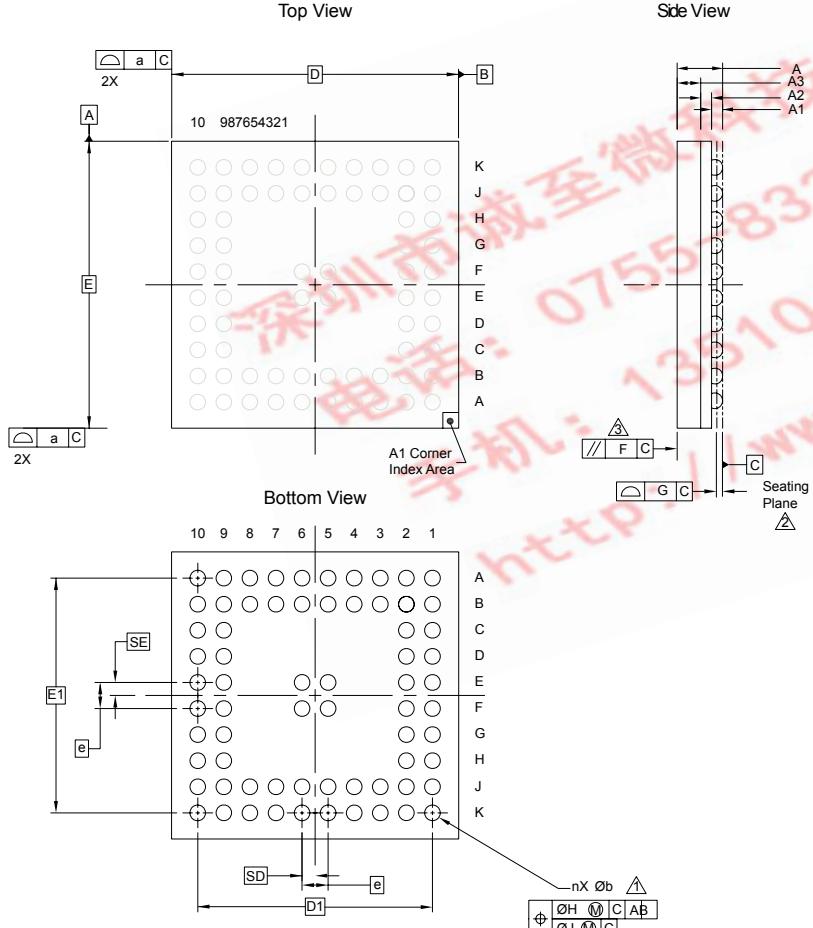
| Codec | Ball | Pad Type | Supply Domain | Description |
|----------|------|--------------|----------------|--|
| MIC_BIAS | B9 | Analogue out | VBAT / 3V3_USB | Microphone bias |
| SPKR_LP | A4 | Analogue out | VDD_AUDIO_DRV | Speaker output positive, left |
| SPKR_LN | B4 | | | Speaker output negative, left |
| SPKR_RP | A6 | Analogue out | VDD_AUDIO_DRV | Speaker output positive, right |
| SPKR_RN | B6 | | | Speaker output negative, right |
| AU_REF | A8 | Analogue in | VDD_AUDIO | Decoupling of audio reference (for high-quality audio) |

| LED Drivers | Ball | Pad Type | Supply Domain | Description |
|-------------|------|---------------|---------------|---|
| LED[2] | B10 | Bidirectional | VDD_PADS_2 | <p>LED driver. Alternative function: programmable output PIO[31]</p> <p>Note: As output is open-drain, an external pull-up is required when PIO[31] is configured as a programmable output.</p> |
| LED[1] | K1 | Bidirectional | VDD_PADS_1 | <p>LED driver. Alternative function: programmable output PIO[30].</p> <p>Note: As output is open-drain, an external pull-up is required when PIO[30] is configured as a programmable output.</p> |
| LED[0] | J2 | Bidirectional | VDD_PADS_1 | <p>LED driver. Alternative function: programmable output PIO[29].</p> <p>Note: As output is open-drain, an external pull-up is required when PIO[29] is configured as a programmable output.</p> |

| Power Supplies and Control | Ball | Description |
|----------------------------|------|--|
| 3V3_USB | J9 | 3.3V bypass linear regulator output. Positive supply for USB port. Connect external minimum 2.2µF ceramic decoupling capacitor. |
| CHG_EXT | J6 | External battery charger control. External battery charger transistor base control when using external charger boost. Otherwise leave unconnected. |
| LX_1V35 | K8 | 1.35V switch-mode power regulator inductor connection. |
| LX_1V8 | K6 | 1.8V switch-mode power regulator inductor connection. |
| SMPS_1V35_SENSE | K10 | 1.35V switch-mode power regulator sense input. |
| SMPS_1V8_SENSE | H9 | 1.8V switch-mode power regulator sense input. |
| VBAT | K7 | Battery positive terminal. |
| VBAT_SENSE | J7 | Battery charger sense input. Connect directly to the battery positive pin. |
| VCHG | K5 | Charger input. Typically connected to VBUS (USB supply) as Section 12 shows. |
| VDD_ANA_RADIO | C2 | Bluetooth radio supply. Connect to 1.35V supply, see Section 12 for connections. |
| VDD_AUDIO | A7 | Positive supply for audio. Connect to 1.35V supply, see Section 12 for connections. |
| VDD_AUDIO_DRV | B5 | Positive supply for audio output amplifiers. Connect to 1.8V supply. |
| VDD_AUX | B2 | Auxiliary supply. Connect to 1.35V supply, see Section 12 for connections. |
| VDD_AUX_1V8 | A1 | Auxiliary LDO regulator input. Connect to 1.8V supply, see Section 12 for connections. |
| VDD_DIG_MEM | K2 | Digital LDO regulator output, see Section 12 for connections. |
| VDD_PADS_1 | E5 | Positive supply input for input/output ports. |
| VDD_PADS_2 | E6 | Positive supply input for input/output ports. |
| VREGENABLE | K4 | Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input. |

| Power Supplies and Control | Ball | Description |
|----------------------------|------|--|
| VREGIN_DIG | K3 | Digital LDO regulator input, see Section 12 for connections. Typically connected to a 1.35V supply. |
| VSS_AUDIO | A5 | Ground connection for audio and audio driver. |
| VSS_BT_LO_AUX | A2 | Ground connections for analogue circuitry and Bluetooth radio local oscillator. |
| VSS_BT_RF | B3 | Bluetooth radio ground. |
| VSS_DIG | F6 | Ground connection for internal digital circuitry. |
| VSS_SMPS_1V35 | K9 | 1.35V switch-mode regulator ground. |
| VSS_SMPS_1V8 | J8 | 1.8V switch-mode regulator ground. |

1.3 Package Dimensions



| Dimension | Min | Typ | Max | Dimension | Min | Typ | Max |
|--------------------|---|------|------|---------------------|--------|-------|-----|
| A | 0.8 | 0.87 | 1.0 | e | - | 0.5 | - |
| A1 | 0.16 | 0.21 | 0.26 | F | - | 0.10 | - |
| A2 | - | 0.21 | - | G | - | 0.08 | - |
| A3 | - | 0.45 | - | H | - | 0.15 | - |
| a | - | 0.05 | - | J | - | 0.08 | - |
| b | 0.27 | 0.32 | 0.37 | n | - | 68 | - |
| D | 5.45 | 5.5 | 5.55 | SD | - | 0.25 | - |
| D1 | - | 4.5 | - | SE | - | 0.25 | - |
| E | 5.45 | 5.5 | 5.55 | Ball diam. | - | 0.3 | - |
| E1 | - | 4.5 | - | Solder land opening | - | 0.275 | - |
| Notes | 1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C. 2. Datum C (seating plane) is defined by the spherical crowns of the solder ball. 3. Parallelism measurement shall exclude any effect of mark on top surface of package. | | | | | | |
| Description | 68-ball Very Thin, Fine Pitch Ball Grid Array (VFBGA) Package | | | | | | |
| Size | 5.5 x 5.5 x 1mm | | | JEDEC | MO-225 | | |
| Pitch | 0.5mm | | | Units | mm | | |

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1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 5.5 x 5.5 x 1mm VFBGA 68-ball package:

- NSMD lands, i.e. lands smaller than the solder mask aperture, are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, use via-in-pad technology to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible, this needs to take into consideration its current carrying and the RF requirements.
- 35 μ m thick (1oz) copper lands are recommended rather than 17 μ m thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be the same as that on the package to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process because this adds to the final volume of solder in the joint, increasing its reliability.
- When using a nickel gold plating finish, the gold thickness should be kept below 0.5 μ m to prevent brittle gold/tin intermetallics forming in the solder.

1.5 Typical Solder Reflow Profile

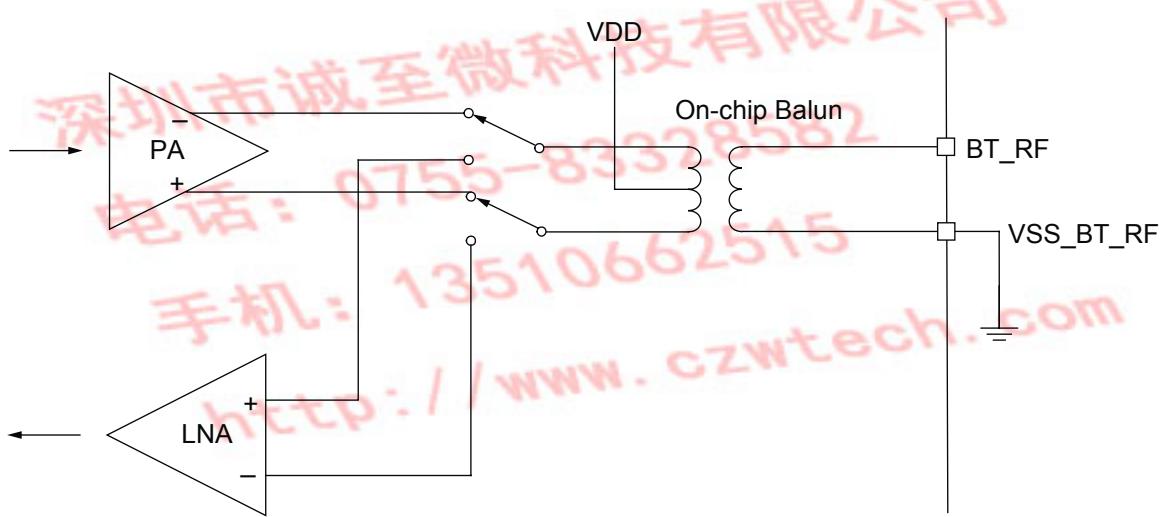
See *Typical Solder Reflow Profile for Lead-free Devices* for information.

2 Bluetooth Modem

2.1 RF Ports

2.1.1 BT_RF

CSR8645 BGA contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power into a 50Ω load.



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Figure 2.1: Simplified Circuit BT_RF

2.2 RF Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. A digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise enables CSR8645 BGA to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the CSR8645 BGA has a maximum output power that enables it to operate as a Class 1, Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.0 specification.

2.5 Baseband

2.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

2.5.2 Physical Layer Hardware Engine

Dedicated logic performs:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

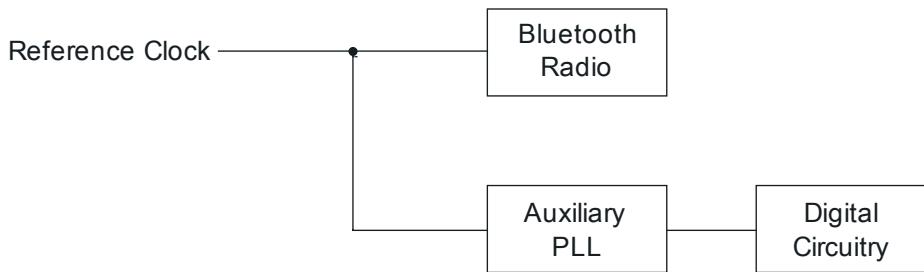
The hardware supports all optional and mandatory features of the Bluetooth v4.0 specification including AFH and eSCO.

3 Clock Generation

CSR8645 BGA requires a Bluetooth reference clock frequency of 16MHz to 32MHz from an externally connected crystal.

All CSR8645 BGA internal digital clocks are generated using a phase locked loop, which is locked to the frequency of the external reference clock source or safely free-runs at a reduced frequency if clock not present.

3.1 Clock Architecture



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Figure 3.1: Clock Architecture

3.2 Input Frequencies and PS Key Settings

CSR8645 BGA is configured to operate with a chosen reference frequency. PSKEY_ANA_FREQ sets this reference frequency for all frequencies using an integer multiple of 250kHz. The input frequency default setting for CSR8645 BGA is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

3.3 Crystal Oscillator: XTAL_IN and XTAL_OUT

CSR8645 BGA contains a crystal driver circuit that acts as a transconductance amplifier driving an external crystal between XTAL_IN and XTAL_OUT. The crystal driver circuit forms a Pierce oscillator with the external crystal. No external crystal load capacitors are required for typical crystals.

3.3.1 Crystal Calibration

The actual crystal frequency depends on the capacitance of XTAL_IN and XTAL_OUT on the PCB and the CSR8645 BGA, as well as the capacitance of the crystal. Correct calibration of the Bluetooth radio is done on a per-device basis on the production line, with the trim value stored in non-volatile memory (PS Key).

Crystal calibration uses a single measurement. The measurement finds the actual offset from the desired frequency and the offset is stored in PSKEY_ANA_FTRIM_OFFSET. The firmware then compensates for the frequency offset on the CSR8645 BGA. Typically, a TXSTART radio test is performed to obtain the actual frequency and it is compared against the output frequency with the requested frequency using an RF analyser. The test station calculates the offset ratio and programs it into PSKEY_ANA_FTRIM_OFFSET. The value in PSKEY_ANA_FTRIM_OFFSET is a 16-bit 2's complement signed integer which specifies the fractional part of the ratio between the true crystal frequency, f_{actual} , and the value set in PSKEY_ANA_FREQ, $f_{nominal}$. Equation 3.1 shows the value of PSKEY_ANA_FTRIM_OFFSET in parts per 2^{20} rounded to the nearest integer.

For more information on TXSTART radio test see *BlueTest User Guide*.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{f_{\text{actual}}}{f_{\text{nominal}}} - 1 \right) \times 2^{20}$$

Equation 3.1: Crystal Calibration Using PSKEY_ANA_FTRIM_OFFSET

For a requested frequency of 2402MHz with an actual output of 2402.0168MHz the PSKEY_ANA_FTRIM_OFFSET value is 7, see Equation 3.2.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{2402.0168}{2402} - 1 \right) \times 2^{20} \approx 7$$

Equation 3.2: Example of PSKEY_ANA_FTRIM_OFFSET Value for 2402.0168MHz

For a requested frequency of 2402MHz with an actual output of 2401.9832MHz the PSKEY_ANA_FTRIM_OFFSET value is -7 (0xffff9), see Equation 3.3.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{2401.9832}{2402} - 1 \right) \times 2^{20} \approx -7$$

Equation 3.3: Example of PSKEY_ANA_FTRIM_OFFSET Value for 2401.9832MHz

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4 Bluetooth Stack Microcontroller

The CSR8645 BGA uses a 16-bit RISC 80MHz MCU for low power consumption and efficient use of memory. It contains a single-cycle multiplier and a memory protection unit for the VM accelerator, see Section 4.1.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

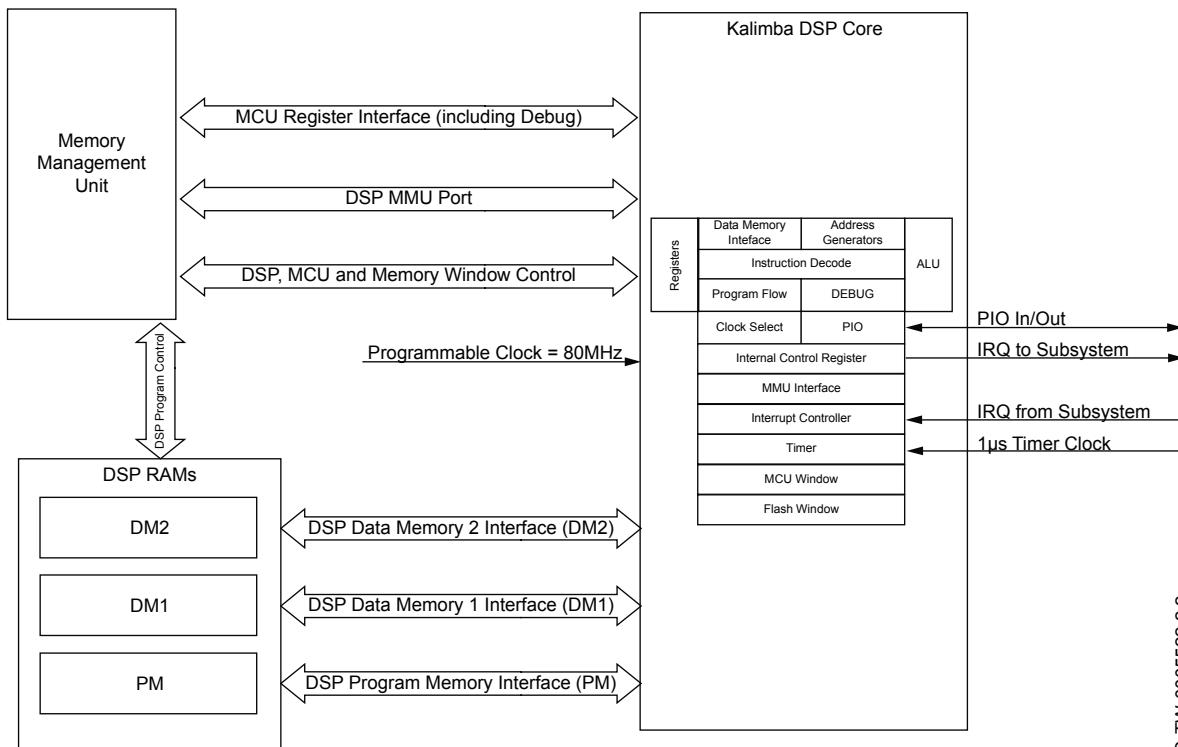
4.1 VM Accelerator

CSR8645 BGA contains a VM accelerator alongside the MCU. This hardware accelerator improves the performance of VM applications.

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5 Kalimba DSP

The Kalimba DSP is an open platform DSP enabling signal processing functions to be performed on over-air data or codec data to enhance audio applications. Figure 5.1 shows the Kalimba DSP interfaces to other functional blocks within CSR8645 BGA.



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Figure 5.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 80MIPS performance, 24-bit fixed point DSP core
- 2 single-cycle MACs; 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to 2 memory accesses in a single cycle
- Zero overhead looping, including a very low-power 32-instruction cache
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 56-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

For more information see *Kalimba Architecture 3 DSP User Guide*.

6 Memory Interface and Management

6.1 Memory Management Unit

The MMU provides dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers. The use of DMA ports also helps with efficient transfer of data to other peripherals.

6.2 System RAM

56KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

6.3 Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 16K x 24-bit for data memory 1 (DM1)
- 16K x 24-bit for data memory 2 (DM2)
- 6K x 32-bit for program memory (PM)

6.4 Internal ROM

Internal ROM is provided for system firmware implementation.

6.5 Serial Flash Interface

CSR8645 BGA supports external serial flash ICs. This enables additional data storage areas for device-specific data. CSR8645 BGA supports serial single I/O devices with a 1-bit I/O flash-memory interface.

Figure 6.1 shows a typical connection between CSR8645 BGA and a serial flash IC.

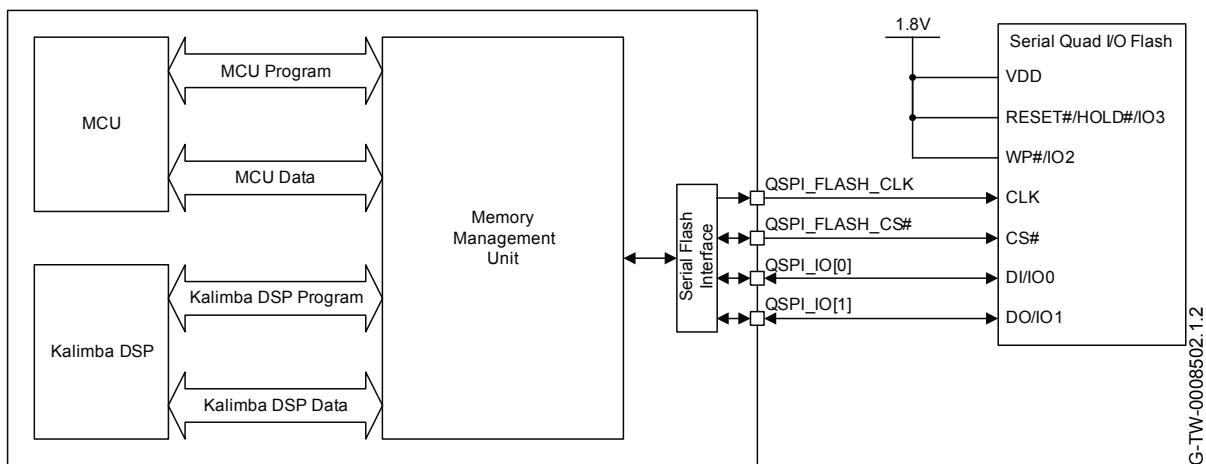


Figure 6.1: Serial Flash Interface

CSR8645 BGA supports Winbond, Microchip/SST, Macronix and compatible serial flash devices for PS Key and voice prompt storage up to 16Mb.

7 Serial Interfaces

7.1 USB Interface

CSR8645 BGA has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on CSR8645 BGA acts as a USB peripheral, responding to requests from a master host controller.

CSR8645 BGA contains internal USB termination resistors and requires no external resistor matching.

CSR8645 BGA supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, supports USB standard charger detection and fully supports the *USB Battery Charging Specification*, available from <http://www.usb.org>. For more information on how to integrate the USB interface on CSR8645 BGA see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
 - Global suspend
 - Selective suspend, includes remote wake
 - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
 - Suspend mode current draw
 - PIO status in suspend mode
 - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

7.2 UART Interface

CSR8645 BGA has one optional standard UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug. The UART interface is multiplexed with PIOs and other functions, and hardware flow control is optional. PS Keys configure this multiplexing, see Table 7.1.

| PS Key | PIO Location Option |
|--------------------|-----------------------------|
| PSKEY_UART_RX_PIO | PIO[0] (default) or PIO[14] |
| PSKEY_UART_TX_PIO | PIO[1] (default) or PIO[15] |
| PSKEY_UART_RTS_PIO | PIO[8] (default) or PIO[16] |
| PSKEY_UART_CTS_PIO | PIO[9] (default) or PIO[17] |

Table 7.1: PS Keys for UART/PIO Multiplexing

Figure 7.1 shows the 4 signals that implement the UART function.

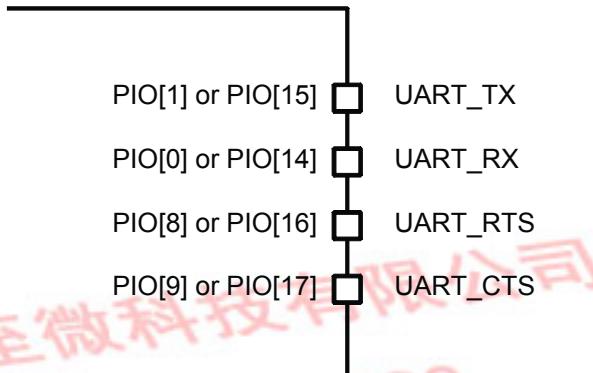


Figure 7.1: Universal Asynchronous Receiver

When CSR8645 BGA is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using CSR8645 BGA firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 7.2 shows the possible UART settings.

| Parameter | Possible Values | |
|---------------------|-------------------|-------------------------------|
| Baud rate | Minimum | 1200 baud ($\leq 2\%$ Error) |
| | | 9600 baud ($\leq 1\%$ Error) |
| | Maximum | 4Mbaud ($\leq 1\%$ Error) |
| Flow control | RTS/CTS or None | |
| Parity | None, Odd or Even | |
| Number of stop bits | 1 or 2 | |
| Bits per byte | 8 | |

Table 7.2: Possible UART Settings

Table 7.3 lists common baud rates and their associated values for the PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range is set in the PS Key according to the formula in Equation 7.1.

$$\text{Baud Rate} = \frac{\text{PSKEY_UART_BAUDRATE}}{0.004096}$$

Equation 7.1: Baud Rate

| Baud Rate | Persistent Store Value | | Error |
|-----------|------------------------|-------|--------|
| | Hex | Dec | |
| 1200 | 0x0005 | 5 | 1.73% |
| 2400 | 0x000a | 10 | 1.73% |
| 4800 | 0x0014 | 20 | 1.73% |
| 9600 | 0x0027 | 39 | -0.82% |
| 19200 | 0x004f | 79 | 0.45% |
| 38400 | 0x009d | 157 | -0.18% |
| 57600 | 0x00ec | 236 | 0.03% |
| 76800 | 0x013b | 315 | 0.14% |
| 115200 | 0x01d8 | 472 | 0.03% |
| 230400 | 0x03b0 | 944 | 0.03% |
| 460800 | 0x075f | 1887 | -0.02% |
| 921600 | 0x0ebf | 3775 | 0.00% |
| 1382400 | 0x161e | 5662 | -0.01% |
| 1843200 | 0x1d7e | 7550 | 0.00% |
| 2764800 | 0x2c3d | 11325 | 0.00% |
| 3686400 | 0x3afb | 15099 | 0.00% |

Table 7.3: Standard Baud Rates

7.3 Programming and Debug Interface

CSR8645 BGA provides a debug SPI interface for programming, configuring (PS Keys) and debugging the CSR8645 BGA. Access to this interface is required in production. Ensure the 4 SPI signals and the SPI/PCM# line are brought out to either test points or a header. To use the SPI interface, the SPI/PCM# line requires the option of being pulled high externally.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

7.3.1 Multi-slave Operation

Avoid connecting CSR8645 BGA in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSR8645 BGA is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, CSR8645 BGA outputs 0 if the processor is running or 1 if it is stopped.

7.4 I²C EEPROM Interface

CSR8645 BGA supports optional I²C EEPROM for storage of PS Keys and voice prompt data if SPI flash is not used. Figure 7.2 shows an example I²C EEPROM connection where:

- PIO[10] is the I²C EEPROM SCL line
- PIO[11] is the I²C EEPROM SDA line
- PIO[12] is the I²C EEPROM WP line

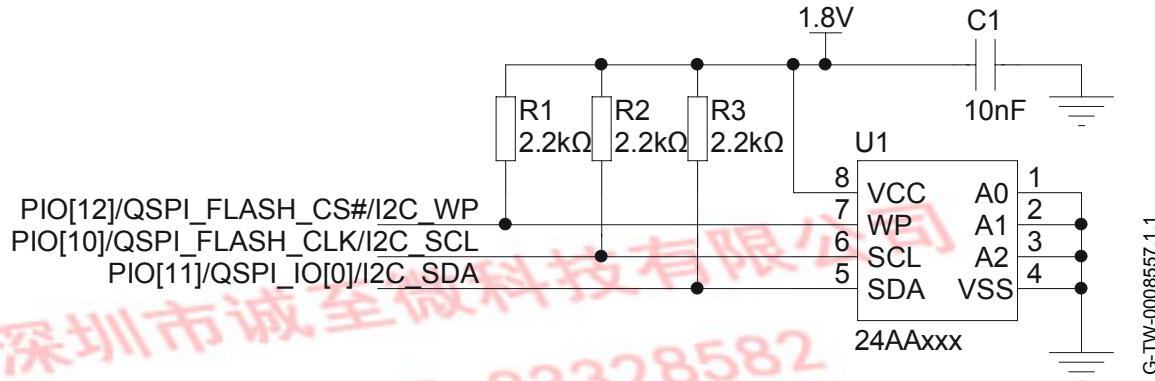


Figure 7.2: Example I²C EEPROM Connection

Note:

The I²C EEPROM requires external pull-up resistors, see Figure 7.2.

CSR recommends 400kHz capable I²C EEPROMs.

8 Interfaces

8.1 Programmable I/O Ports, PIO

CSR8645 BGA provides 22 lines of programmable bidirectional I/O, PIO[21:0]. Some of the PIOs on the CSR8645 BGA have alternative functions, see Table 8.1.

| PIO | Function | | | | |
|---------|--------------------------------|--------------------------------|---------------------------|--------------------------|-----------------------------|
| | Debug SPI (See Section 7.3) | SPI Flash (See Section 6.5) | UART (See Section 7.2) | PCM (See Section 9.3) | EEPROM (See Section 7.4) |
| PIO[0] | - | - | UART_RX (default) | - | - |
| PIO[1] | - | - | UART_TX (default) | - | - |
| PIO[2] | SPI_MOSI | - | - | PCM1_IN | - |
| PIO[3] | SPI_MISO | - | - | PCM1_OUT | - |
| PIO[4] | SPI_CS# | - | - | PCM1_SYNC | - |
| PIO[5] | SPI_CLK | - | - | PCM1_CLK | - |
| PIO[8] | - | - | UART_RTS (default) | - | - |
| PIO[9] | - | - | UART_CTS (default) | - | - |
| PIO[10] | - | QSPI_FLASH_CLK | - | - | I2C_SCL |
| PIO[11] | - | QSPI_IO[0] | - | - | I2C_SDA |
| PIO[12] | - | QSPI_FLASH_CS# | - | - | I2C_WP |
| PIO[13] | - | QSPI_IO[1] | - | - | - |
| PIO[14] | - | - | UART_RX | - | - |
| PIO[15] | - | - | UART_TX | - | - |
| PIO[16] | - | - | UART_RTS | - | - |
| PIO[17] | - | - | UART_CTS | - | - |

Table 8.1: Alternative PIO Functions

Note:

See the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

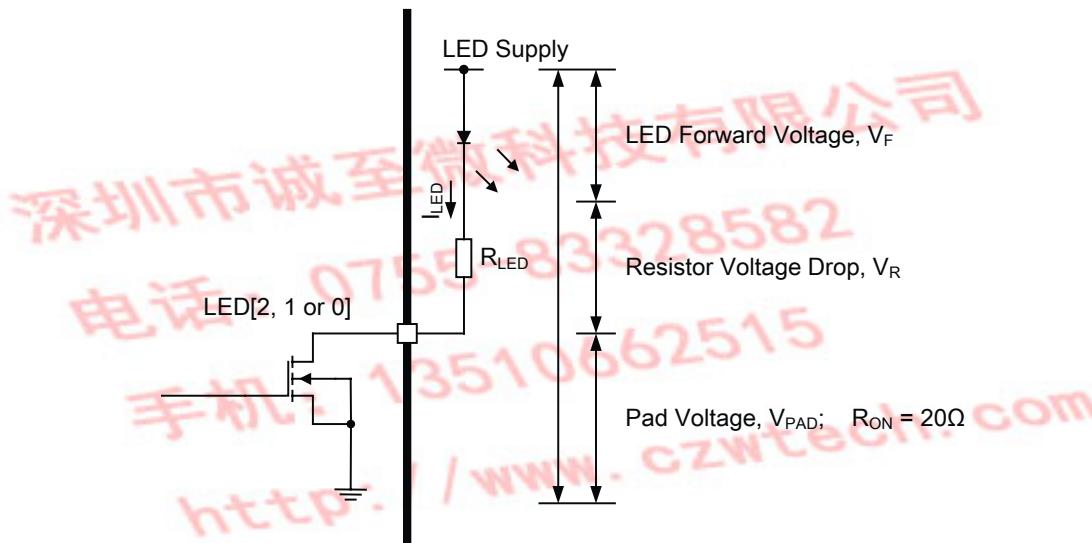
8.2 Analogue I/O Ports, AIO

CSR8645 BGA has 1 general-purpose analogue interface pin, AIO[0]. Typically, this connects to a thermistor for battery pack temperature measurements during charge control. See Section 12 for typical connections.

8.3 LED Drivers

CSR8645 BGA includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.



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Figure 8.1: LED Equivalent Circuit

From Figure 8.1 it is possible to derive Equation 8.1 to calculate I_{LED} . If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{V_{DD} - V_F}{R_{LED} + R_{ON}}$$

Equation 8.1: LED Current

For the LED pads to act as resistance, the external series resistor, R_{LED} , needs to be such that the voltage drop across it, V_R , keeps V_{PAD} below 0.5V. Equation 8.2 also applies.

$$V_{DD} = V_F + V_R + V_{PAD}$$

Equation 8.2: LED PAD Voltage

Note:

The supply domain in Section 1.2 for LED[2:0] must remain powered for LED functions to operate.

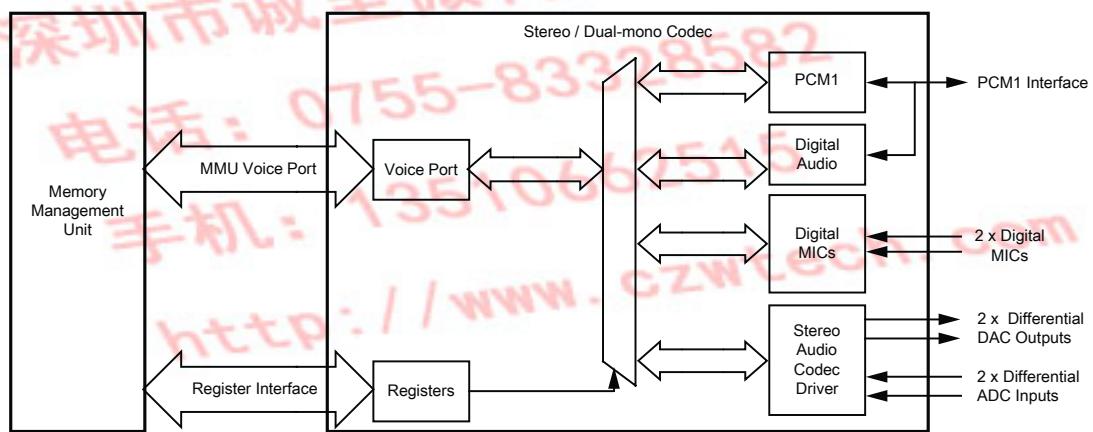
The LED current adds to the overall current. Conservative LED selection extends battery life.

9 Audio Interface

The audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analogue audio inputs
- Dual analogue audio outputs
- 2 digital microphone inputs
- Configurable PCM (PCM1) and I²S interfaces, for configuration information contact CSR

Figure 9.1 shows the functional blocks of the interface. The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC and the DAC of the codec each contain 2 independent high-quality channels. Any ADC or DAC channel runs at its own independent sample rate.



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Figure 9.1: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM1 codec interface described in Section 9.3. Table 9.1 lists the alternative functions.

Important Note:

The term *PCM* in Section 9.3 and its subsections refers to the PCM1 interface.

| PCM Interface | I ² S Interface |
|---------------|----------------------------|
| PCM_OUT | SD_OUT |
| PCM_IN | SD_IN |
| PCM_SYNC | WS |
| PCM_CLK | SCK |

Table 9.1: Alternative Functions of the Digital Audio Bus Interface on the PCM1 Interface

9.1 Audio Input and Output

The audio input circuitry consists of:

- 2 independent 16-bit high-quality ADC channels:
 - Programmable as either microphone or line input
 - Programmable as either stereo or dual-mono inputs
 - Multiplexed with 1 of the digital microphone inputs, see Figure 9.2 and Section 9.2.14
 - Each channel is independently configurable to be either single-ended or fully differential
 - Each channel has an analogue and digital programmable gain stage for optimisation of different microphones
- 2 digital microphone inputs (MEMS)

The audio output circuitry consists of a dual differential class A-B output stage.

Note:

CSR8645 BGA is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

9.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for I²S stereo digital audio bus standard
- Support for PCM interface including PCM master codecs that require an external system clock

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio output. With respect to audio input, software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

9.2.1 Audio Codec Block Diagram

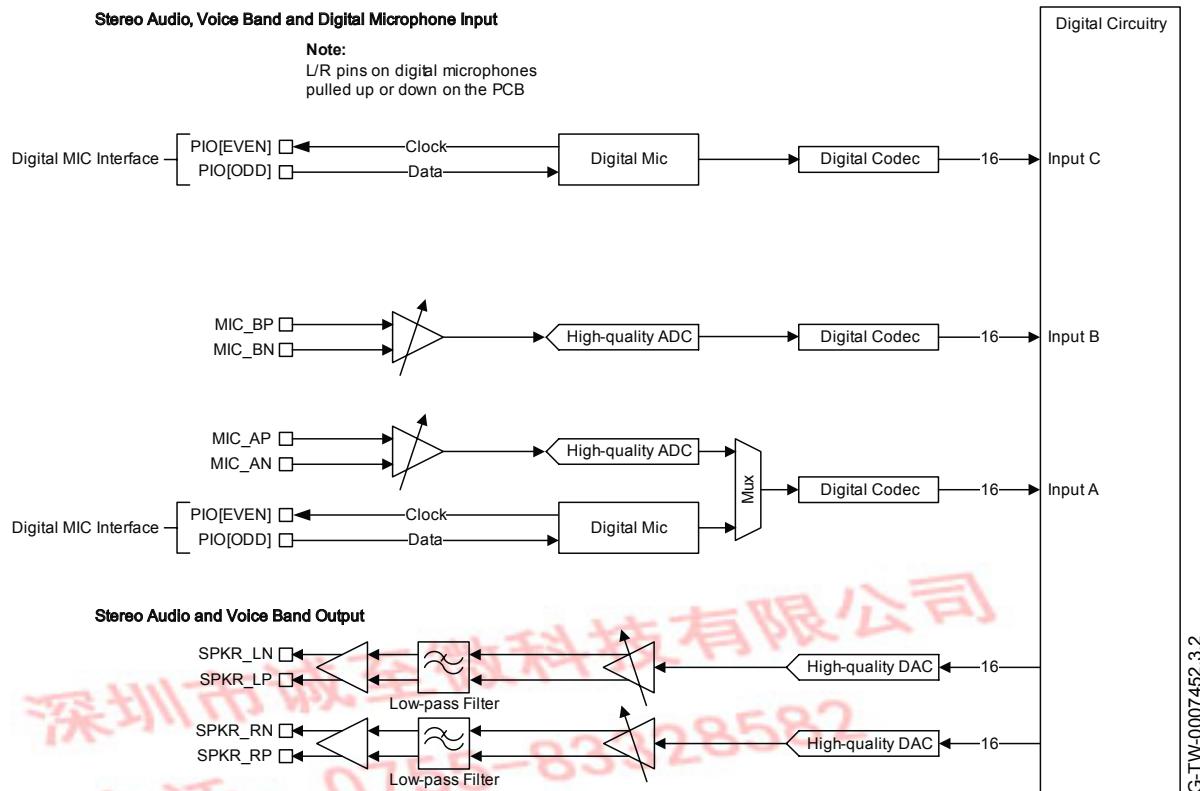


Figure 9.2: Audio Codec Input and Output Stages

The CSR8645 BGA audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO for the audio circuits and VDD_AUDIO_DRV for the audio driver circuits.

9.2.2 ADC

Figure 9.2 shows the CSR8645 BGA consists of 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage, see Section 9.2.4.

9.2.3 ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40kHz:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz

9.2.4 ADC Audio Input Gain

Figure 9.3 shows that the CSR8645 BGA audio input gain consists of:

- An analogue gain stage based on a pre-amplifier and an analogue gain amplifier, see Section 9.2.5
- A digital gain stage, see Section 9.2.6

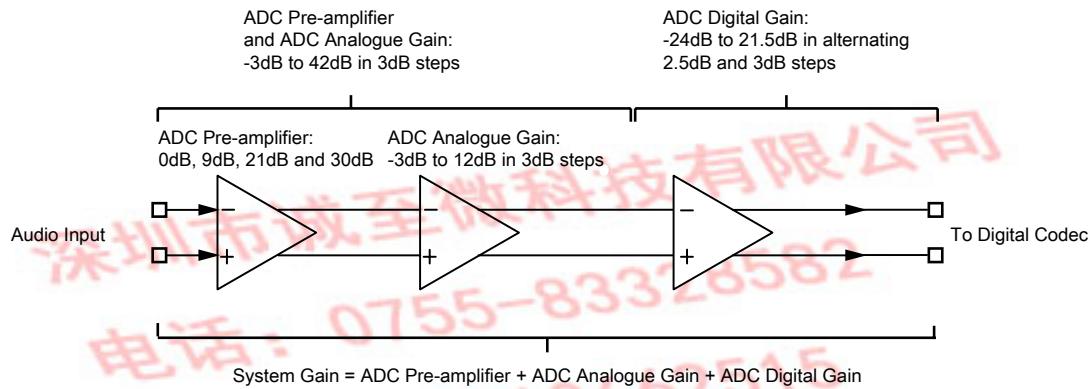


Figure 9.3: Audio Input Gain

9.2.5 ADC Pre-amplifier and ADC Analogue Gain

CSR8645 BGA has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0dB, 9dB, 21dB and 30dB
- The ADC analogue amplifier gain is -3dB to 12dB in 3dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3dB to 42dB in 3dB steps, see Figure 9.3
- At mid to high gain levels it acts as a microphone pre-amplifier, see Section 9.2.13
- At low gain levels it acts as an audio line level amplifier

9.2.6 ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see Table 9.2. There is also a *fine gain interface* with a 9-bit gain setting allowing gain changes in 1/32 steps, for more information contact CSR.

The firmware controls the audio input gain.

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| Digital Gain Selection Value | ADC Digital Gain Setting (dB) | Digital Gain Selection Value | ADC Digital Gain Setting (dB) |
|------------------------------|-------------------------------|------------------------------|-------------------------------|
| 0 | 0 | 8 | -24 |
| 1 | 3.5 | 9 | -20.5 |
| 2 | 6 | 10 | -18 |
| 3 | 9.5 | 11 | -14.5 |
| 4 | 12 | 12 | -12 |
| 5 | 15.5 | 13 | -8.5 |
| 6 | 18 | 14 | -6 |
| 7 | 21.5 | 15 | -2.5 |

Table 9.2: ADC Audio Input Gain Rate

9.2.7 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A *long* IIR filter suitable for music (>44.1kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8kHz / 16kHz / voice)

For more information contact CSR.

9.2.8 DAC

The DAC consists of:

- 2 fourth-order Sigma-Delta converters enabling 2 separate channels that are identical in functionality, as Figure 9.2 shows.
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage.

9.2.9 DAC Sample Rate Selection

Each DAC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 32kHz
- 40kHz
- 44.1kHz
- 48kHz
- 96kHz

9.2.10 DAC Digital Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB, see Table 9.3. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact CSR.

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

| Digital Gain Selection Value | DAC Digital Gain Setting (dB) | Digital Gain Selection Value | DAC Digital Gain Setting (dB) |
|------------------------------|-------------------------------|------------------------------|-------------------------------|
| 0 | 0 | 8 | -24 |
| 1 | 3.5 | 9 | -20.5 |
| 2 | 6 | 10 | -18 |
| 3 | 9.5 | 11 | -14.5 |
| 4 | 12 | 12 | -12 |
| 5 | 15.5 | 13 | -8.5 |
| 6 | 18 | 14 | -6 |
| 7 | 21.5 | 15 | -2.5 |

Table 9.3: DAC Digital Gain Rate Selection

9.2.11 DAC Analogue Gain

Table 9.4 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

| Analogue Gain Selection Value | DAC Analogue Gain Setting (dB) | Analogue Gain Selection Value | DAC Analogue Gain Setting (dB) |
|-------------------------------|--------------------------------|-------------------------------|--------------------------------|
| 7 | 0 | 3 | -12 |
| 6 | -3 | 2 | -15 |
| 5 | -6 | 1 | -18 |
| 4 | -9 | 0 | -21 |

Table 9.4: DAC Analogue Gain Rate Selection

9.2.12 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default *long* FIR filter for best performance at $\geq 44.1\text{kHz}$.
- A *short* FIR to reduce latency.
- A *narrow* FIR (a very sharp roll-off at Nyquist) for G.722 compliance. Best for 8kHz / 16kHz.

9.2.13 Microphone Input

CSR8645 BGA contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condenser microphones. Figure 9.4 shows a biasing circuit for microphones with a sensitivity between about -40 to -60dB (0dB = 1V/Pa).

Where:

- The microphone bias generator derives its power from VBAT or 3V3_USB and requires no capacitor on its output.
- The microphone bias generator maintains regulation within the limits 70 μ A to 2.8mA, supporting a 2mA source typically required by 2 electret condenser microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
- Biasing resistors R1 and R2 equal 2.2k Ω .
- The input impedance at MIC_AN, MIC_AP, MIC_BP and MIC_BN is typically 6k Ω .
- C1, C2, C3 and C4 are 100/150nF if bass roll-off is required to limit wind noise on the microphone.
- R1 and R2 set the microphone load impedance and are normally around 2.2k Ω .

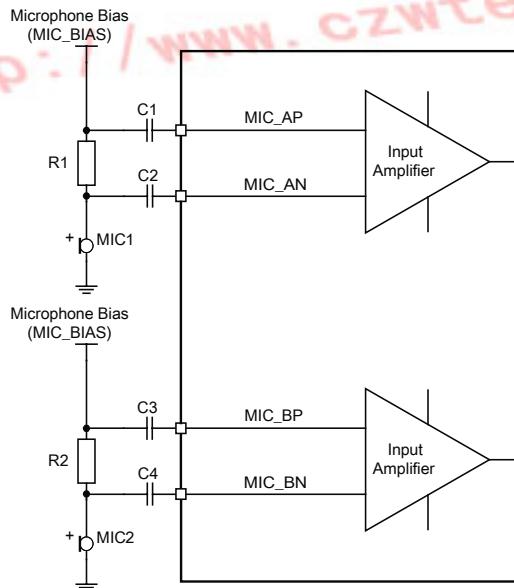


Figure 9.4: Microphone Biasing

The microphone bias characteristics include:

- Power supply:
 - CSR8645 BGA microphone supply is VBAT or 3V3_USB
 - Minimum input voltage = Output voltage + drop-out voltage
 - Maximum input voltage is 4.3V
- Drop-out voltage:
 - 300mV maximum
- Output voltage:
 - 1.8V or 2.6V
 - Tolerance 90% to 110%
- Output current:
 - 70 μ A to 2.8mA
- No load capacitor required

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9.2.14 Digital Microphone Inputs

The CSR8645 BGA interfaces to 2 digital microphone inputs. Figure 9.2 shows the interface between the codec and the digital microphone interface. Figure 9.2 shows that the digital microphone interface on the CSR8645 BGA has:

- Clock lines linked to any even-numbered PIO as determined by the firmware.
- Data lines linked to any odd-numbered PIO as determined by the firmware.

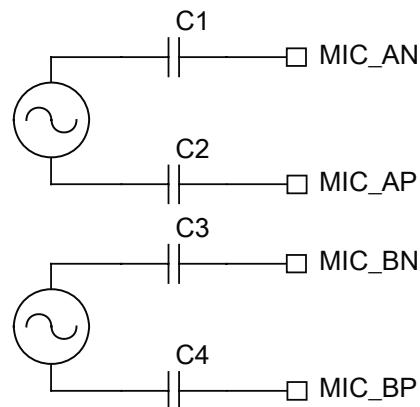
Note:

For the digital microphone interface to work in this configuration ensure the microphone uses a tristate between edges.

- The left and right selection for the digital microphones are appropriately pulled up or down for selection on the PCB.

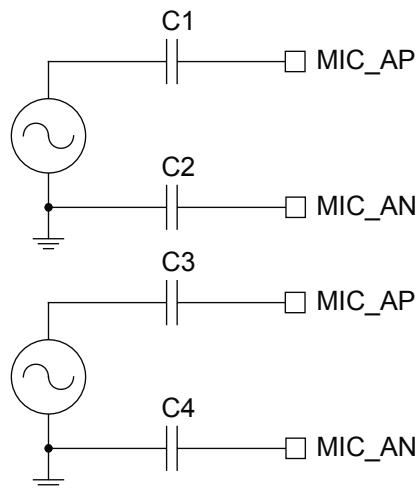
9.2.15 Line Input

Section 9.2.4 states that if the pre-amplifier audio input gain is set at a low gain level it acts as an audio line level amplifier. In this line input mode the input impedance varies from $6\text{k}\Omega$ to $30\text{k}\Omega$, depending on the volume setting. Figure 9.5 and Figure 9.6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.



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Figure 9.5: Differential Input



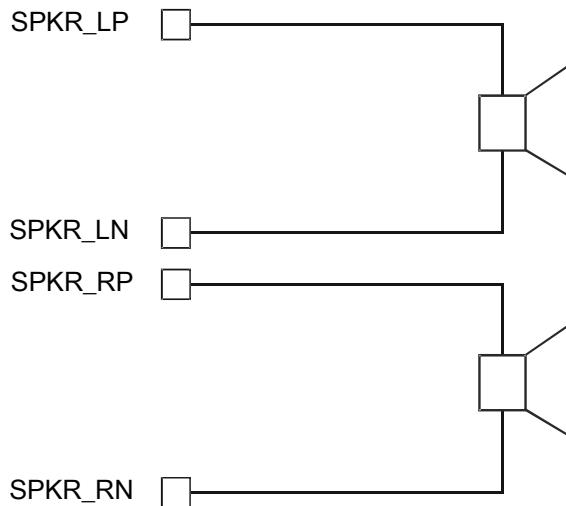
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Figure 9.6: Single-ended Input

9.2.16 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 9.7 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.



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Figure 9.7: Speaker Output

9.2.17 Mono Operation

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

9.2.18 Side Tone

In some applications it is necessary to implement side tone. This side tone function involves feeding a properly gained microphone signal in to the DAC stream, e.g. earpiece. The side tone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface, see Figure 9.8.

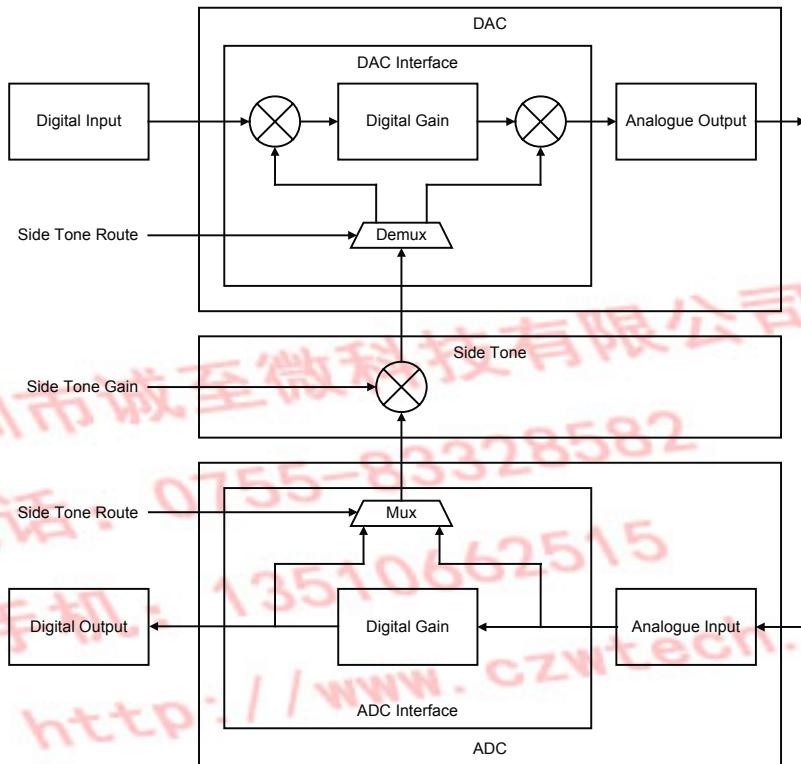


Figure 9.8: Side Tone

The ADC provides simple gain to the side tone data. The gain values range from -32.6dB to 12.0dB in alternating steps of 2.5dB and 3.5dB, see Table 9.5.

| Value | Side Tone Gain | Value | Side Tone Gain |
|-------|----------------|-------|----------------|
| 0 | -32.6dB | 8 | -8.5dB |
| 1 | -30.1dB | 9 | -6.0dB |
| 2 | -26.6dB | 10 | -2.5dB |
| 3 | -24.1dB | 11 | 0dB |
| 4 | -20.6dB | 12 | 3.5dB |
| 5 | -18.1dB | 13 | 6.0dB |
| 6 | -14.5dB | 14 | 9.5dB |
| 7 | -12.0dB | 15 | 12.0dB |

Table 9.5: Side Tone Gain

Note:

The values of side tone are shown for information only. During standard operation, the application software controls the side tone gain.

The following PS Keys configure the side tone hardware:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

9.2.19 Integrated Digital IIR Filter

CSR8645 BGA has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2-stage, second order IIR and is for functions such as custom wind noise reduction. The filter also has optional DC blocking.

The filter has 10 configuration words:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format NN.NNNNNNNNNN.

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

| | |
|---------------|------------------------------------|
| 01.1111111111 | = most positive number, close to 2 |
| 01.0000000000 | = 1 |
| 00.0000000000 | = 0 |
| 11.0000000000 | = -1 |
| 10.0000000000 | = -2, most negative number |

Equation 9.1 shows the equation for the IIR filter. Equation 9.2 shows the equation for when the DC blocking is enabled.

The filter is configured, enabled and disabled from the VM via the CodecSetIIRFilterA and CodecSetIIRFilterB traps. This requires firmware support. The configuration function takes 10 variables in the following order:

| | | |
|---|---|----------|
| 0 | : | Gain |
| 1 | : | b_{01} |
| 2 | : | b_{02} |
| 3 | : | a_{01} |
| 4 | : | a_{02} |
| 5 | : | b_{11} |
| 6 | : | b_{12} |
| 7 | : | a_{11} |
| 8 | : | a_{12} |
| 9 | : | a_{12} |

DC Block (1 = enable, 0 = disable)

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01} z^{-1} + b_{02} z^{-2})}{(1 + a_{01} z^{-1} + a_{02} z^{-2})} \times \frac{(1 + b_{11} z^{-1} + b_{12} z^{-2})}{(1 + a_{11} z^{-1} + a_{12} z^{-2})}$$

Equation 9.1: IIR Filter Transfer Function, $H(z)$

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 9.2: IIR Filter Plus DC Blocking Transfer Function, $H_{DC}(z)$

9.3 PCM1 Interface

Section 9 describes the various digital audio interfaces multiplexed on the the PCM1 interface. The PCM1 interface also shares the same physical set of pins with the SPI interface, see Section 7.3 and Section 8.1. Either interface is selected using SPI_PCM#:

- SPI_PCM# = 1 selects SPI
- SPI_PCM# = 0 selects PCM

Important Note:

The term *PCM* refers to PCM1.

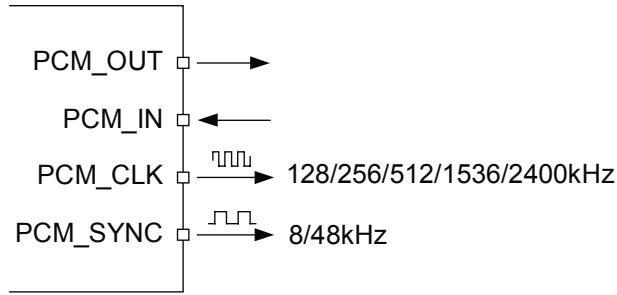
The audio PCM interface on the CSR8645 BGA supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the CSR8645 BGA for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
 - Long Frame Sync
 - Short Frame Sync
 - GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ -law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PSKEY_PCM_CONFIG32.

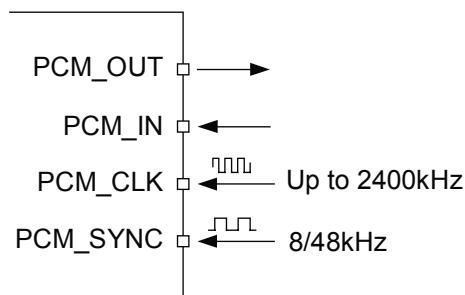
9.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSR8645 BGA generates PCM_CLK and PCM_SYNC.



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Figure 9.9: PCM Interface Master



G-TW-00002183.3

Figure 9.10: PCM Interface Slave

9.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When CSR8645 BGA is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When CSR8645 BGA is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

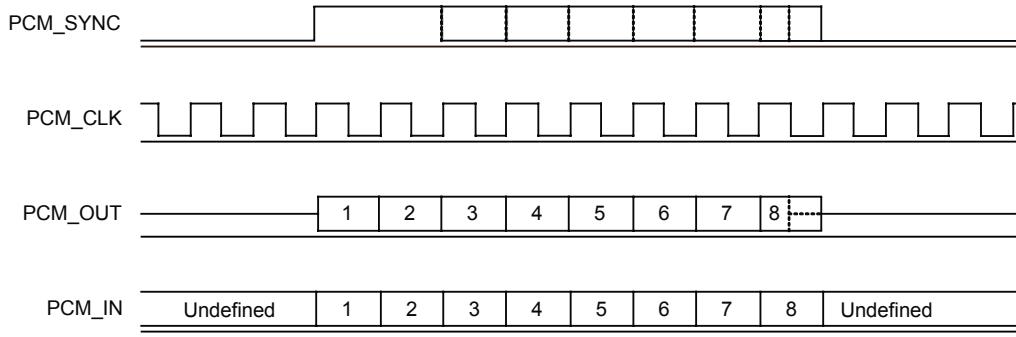


Figure 9.11: Long Frame Sync (Shown with 8-bit Companded Sample)

CSR8645 BGA samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always 1 clock cycle long.

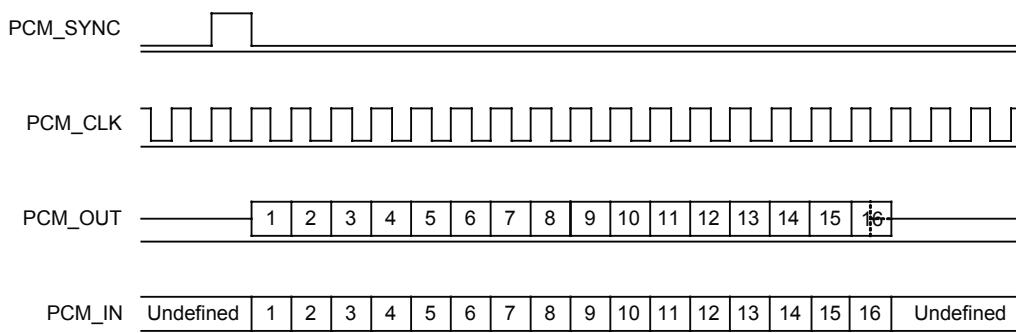


Figure 9.12: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, CSR8645 BGA samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.3.4 Multi-slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any of the first 4 slots.

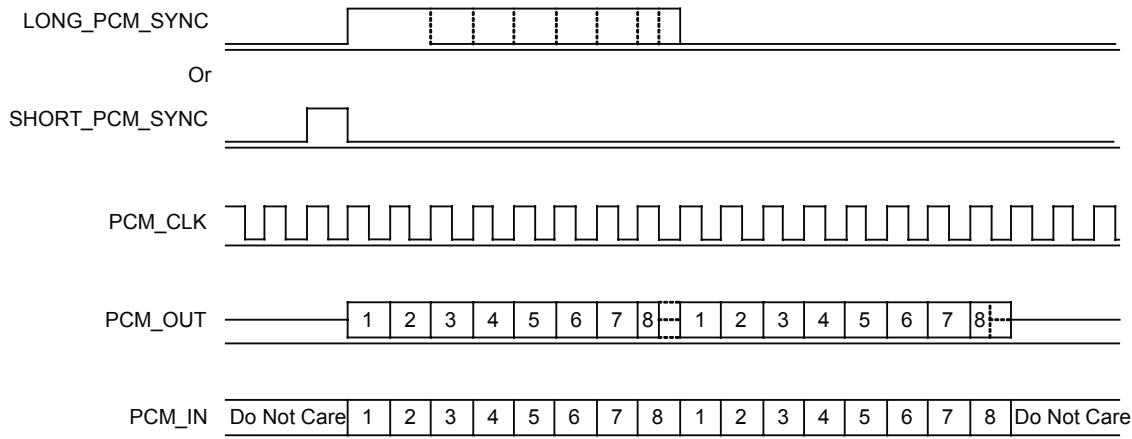


Figure 9.13: Multi-slot Operation with 2 Slots and 8-bit Companded Samples

9.3.5 GCI Interface

CSR8645 BGA is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels are accessed when this mode is configured.

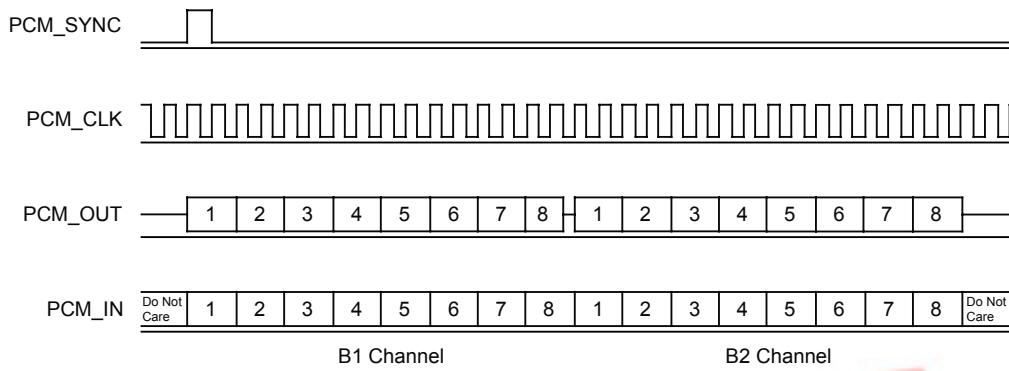


Figure 9.14: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

9.3.6 Slots and Sample Formats

CSR8645 BGA receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

CSR8645 BGA supports:

- 13-bit linear, 16-bit linear and 8-bit μ -law or A-law sample formats.
- A sample rate of 8ksps.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

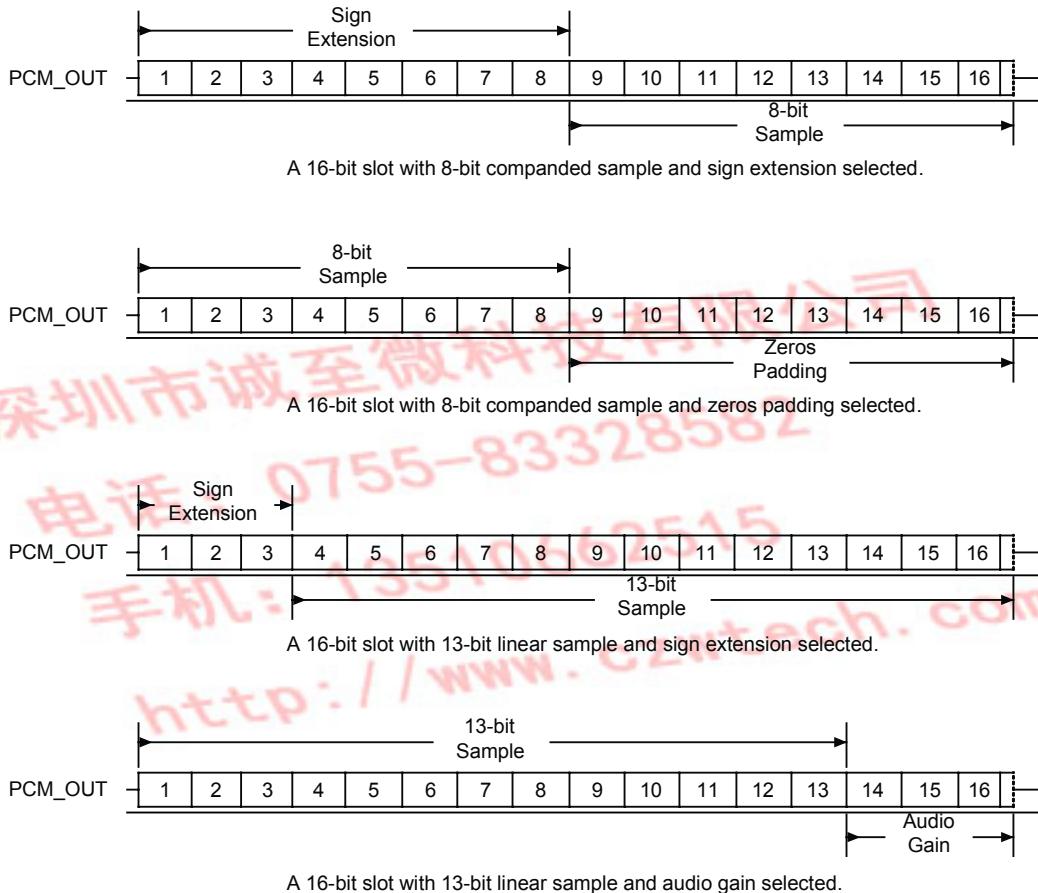


Figure 9.15: 16-bit Slot Length and Sample Formats

9.3.7 Additional Features

CSR8645 BGA has a mute facility that forces PCM_OUT to be 0. In master mode, CSR8645 BGA is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

9.3.8 PCM Timing Information

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-------------------|--|---|----------------------|-----|-----|----------|
| f_{mclk} | PCM_CLK frequency | 4MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10. | - | 128 | - | kHz |
| | | 48MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10. | | 256 | | |
| | | 48MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10. | | 512 | | |
| - | PCM_SYNC frequency for SCO connection | | 2.9 | - | - | kHz |
| t_{mclkh} (a) | PCM_CLK high | 4MHz DDS generation | 980 | - | - | ns |
| t_{mclk1} (a) | PCM_CLK low | 4MHz DDS generation | 730 | - | - | ns |
| - | PCM_CLK jitter | | 48MHz DDS generation | - | 21 | ns pk-pk |
| $t_{dmclksynch}$ | Delay time from PCM_CLK high to PCM_SYNC high | | - | - | 20 | ns |
| $t_{dmclkpout}$ | Delay time from PCM_CLK high to valid PCM_OUT | | - | - | 20 | ns |
| $t_{dmclklsyncl}$ | Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only) | | - | - | 20 | ns |
| $t_{dmclkhsyncl}$ | Delay time from PCM_CLK high to PCM_SYNC low | | - | - | 20 | ns |
| $t_{dmclklpoutz}$ | Delay time from PCM_CLK low to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{dmclkhpoutz}$ | Delay time from PCM_CLK high to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{supinclk1}$ | Set-up time for PCM_IN valid to PCM_CLK low | | 20 | - | - | ns |
| $t_{hpinclk1}$ | Hold time for PCM_CLK low to PCM_IN invalid | | 0 | - | - | ns |

Table 9.6: PCM Master Timing

(a) Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

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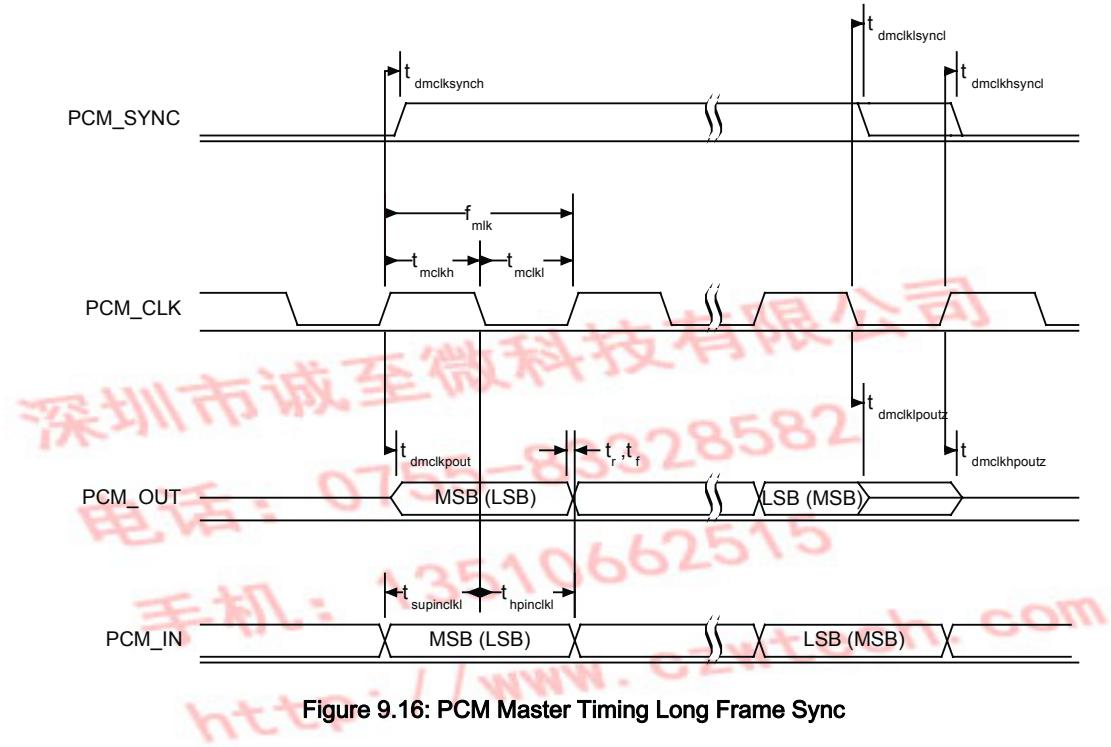


Figure 9.16: PCM Master Timing Long Frame Sync

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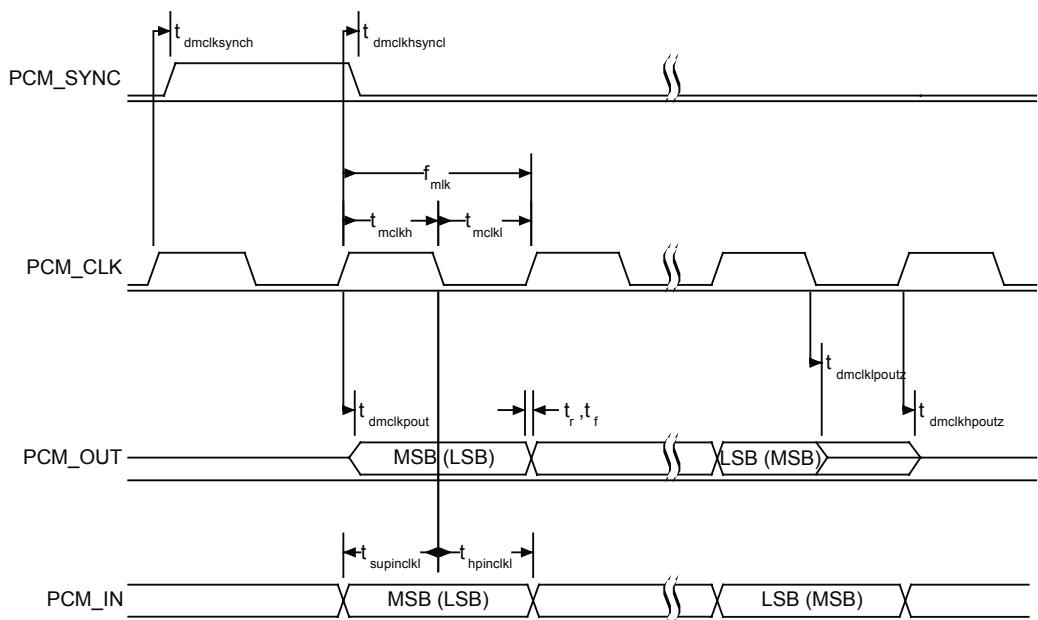


Figure 9.17: PCM Master Timing Short Frame Sync

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|---|-----|-----|-----|------|
| f_{sclk} | PCM clock frequency (Slave mode: input) | 64 | - | (a) | kHz |
| f_{sclk} | PCM clock frequency (GCI mode) | 128 | - | (b) | kHz |
| t_{sclkl} | PCM_CLK low time | 200 | - | - | ns |
| t_{sclkh} | PCM_CLK high time | 200 | - | - | ns |
| $t_{hsclksynch}$ | Hold time from PCM_CLK low to PCM_SYNC high | 2 | - | - | ns |
| $t_{susclksynch}$ | Set-up time for PCM_SYNC high to PCM_CLK low | 20 | - | - | ns |
| t_{dpout} | Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long Frame Sync only) | - | - | 20 | ns |
| $t_{dsclkhpout}$ | Delay time from CLK high to PCM_OUT valid data | - | - | 15 | ns |
| t_{dpoutz} | Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance | - | - | 15 | ns |
| $t_{supinsclkI}$ | Set-up time for PCM_IN valid to CLK low | 20 | - | - | ns |
| $t_{hpinsclkI}$ | Hold time for PCM_CLK low to PCM_IN invalid | 2 | - | - | ns |

Table 9.7: PCM Slave Timing

(a) Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

(b) Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

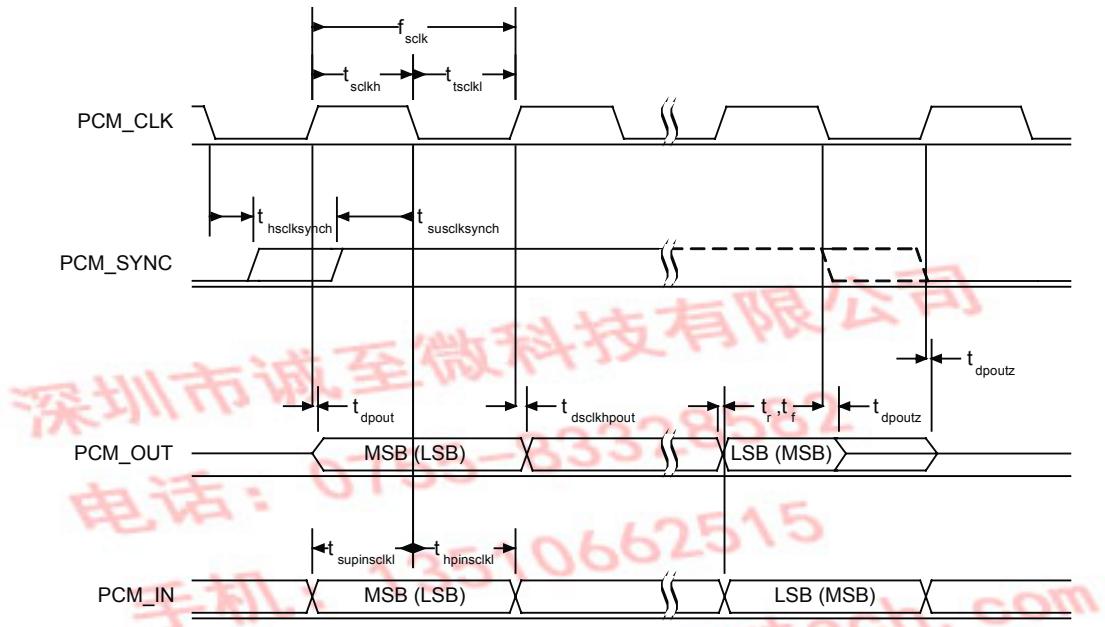


Figure 9.18: PCM Slave Timing Long Frame Sync

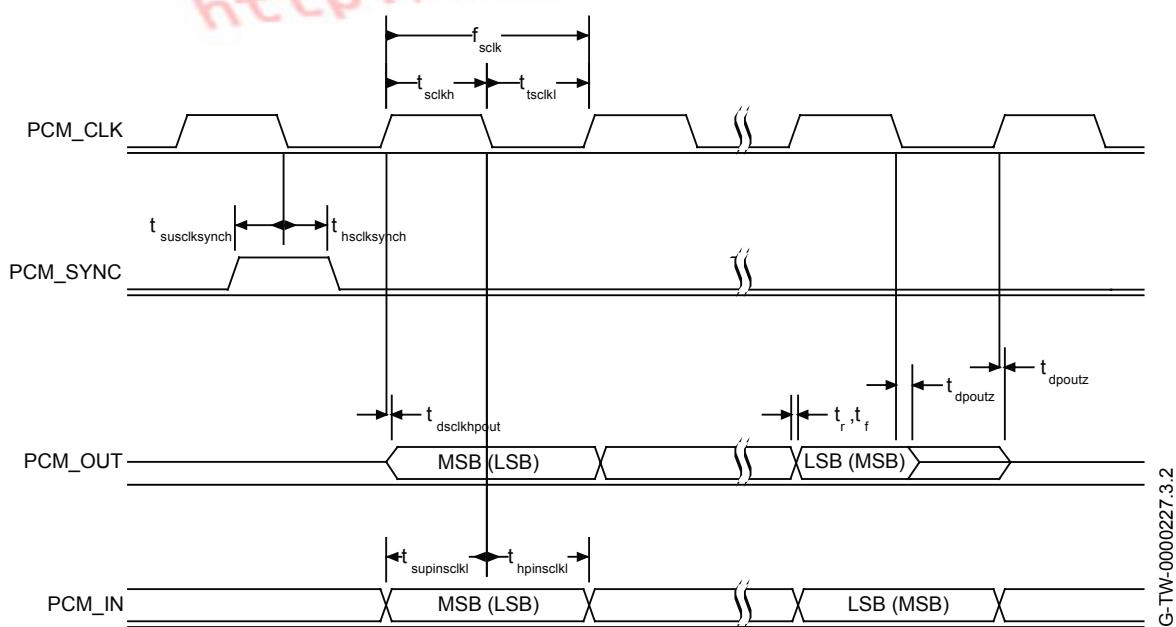


Figure 9.19: PCM Slave Timing Short Frame Sync

9.3.9 PCM_CLK and PCM_SYNC Generation

CSR8645 BGA has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from CSR8645 BGA internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock (which enables a greater range of frequencies to be generated with low jitter but consumes more power). To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 9.3 describes PCM_CLK frequency when generated from the internal 48MHz clock:

$$f = \frac{\text{CNT_RATE}}{\text{CNT_LIMIT}} \times 24\text{MHz}$$

Equation 9.3: PCM_CLK Frequency Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 9.4:

$$f = \frac{\text{PCM_CLK}}{\text{SYNC_LIMIT} \times 8}$$

Equation 9.4: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_USE_LOW_JITTER_MODE.

9.3.10 PCM Configuration

Configure the PCM by using PSKEY_PCM_CONFIG32 and PSKEY_PCM_USE_LOW_JITTER_MODE, see *BlueCore Audio API Specification* and the PS Key file. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

9.4 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 9.8 lists these alternative functions. Figure 9.20 shows the timing diagram.

| PCM Interface | I ² S Interface |
|---------------|----------------------------|
| PCM_OUT | SD_OUT |
| PCM_IN | SD_IN |
| PCM_SYNC | WS |
| PCM_CLK | SCK |

Table 9.8: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see *BlueCore Audio API Specification* and the PS Key file.

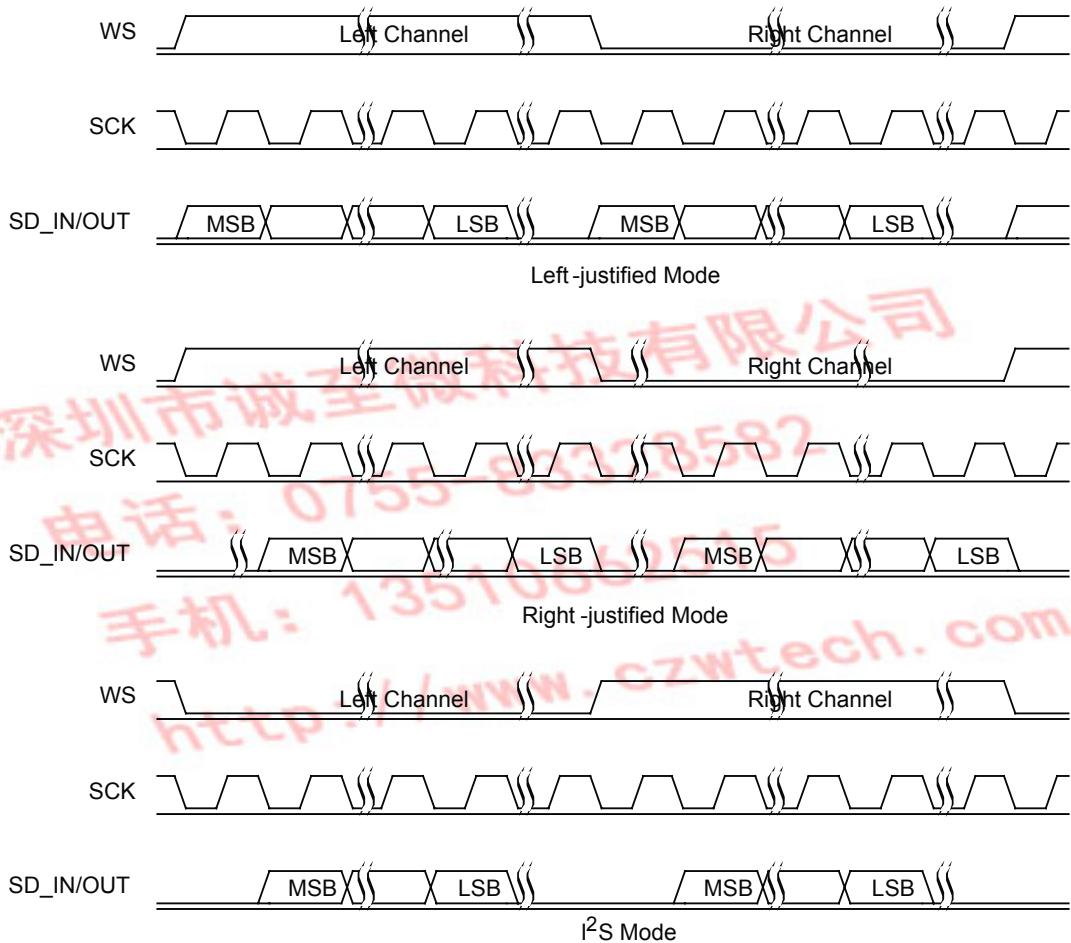


Figure 9.20: Digital Audio Interface Modes

The internal representation of audio samples within CSR8645 BGA is 16-bit and data on SD_OUT is limited to 16-bit per channel.

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------|---------------|-----|-----|-----|------|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |
| t_{ch} | SCK high time | 80 | - | - | ns |
| t_{cl} | SCK low time | 80 | - | - | ns |

Table 9.9: Digital Audio Interface Slave Timing

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| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|-------------------------------------|-----|-----|-----|------|
| t_{ssu} | WS valid to SCK high set-up time | 20 | - | - | ns |
| t_{sh} | SCK high to WS invalid hold time | 2.5 | - | - | ns |
| t_{opd} | SCK low to SD_OUT valid delay time | - | - | 20 | ns |
| t_{isu} | SD_IN valid to SCK high set-up time | 20 | - | - | ns |
| t_{ih} | SCK high to SD_IN invalid hold time | 2.5 | - | - | ns |

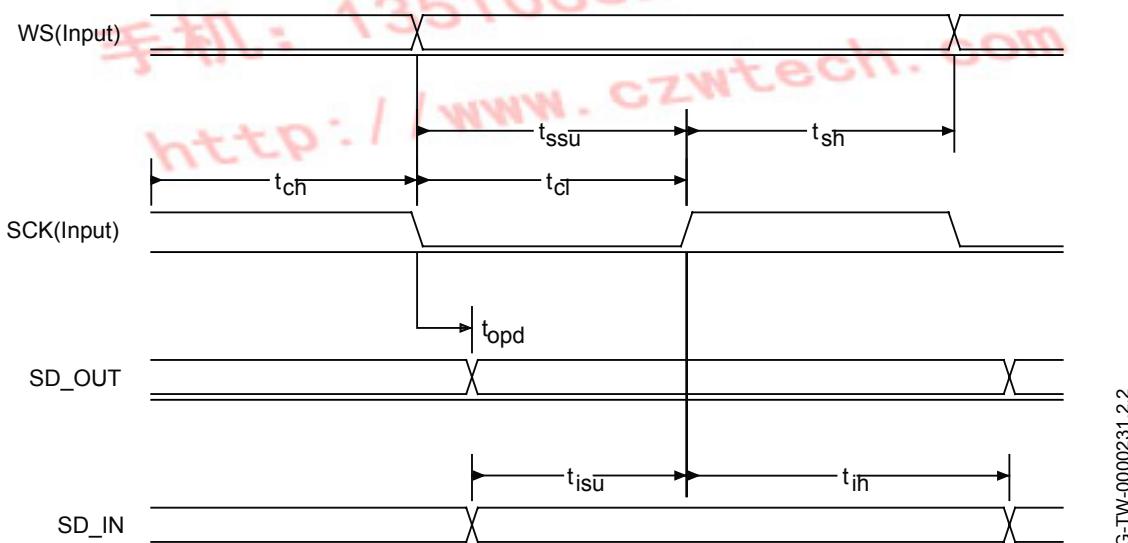
 Table 9.10: I²S Slave Mode Timing


Figure 9.21: Digital Audio Interface Slave Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|---------------|-----|-----|-----|------|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |

Table 9.11: Digital Audio Interface Master Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|-------------------------------------|-------|-----|-------|------|
| t_{spd} | SCK low to WS valid delay time | - | - | 39.27 | ns |
| t_{opd} | SCK low to SD_OUT valid delay time | - | - | 18.44 | ns |
| t_{isu} | SD_IN valid to SCK high set-up time | 18.44 | - | - | ns |
| t_{ih} | SCK high to SD_IN invalid hold time | 0 | - | - | ns |

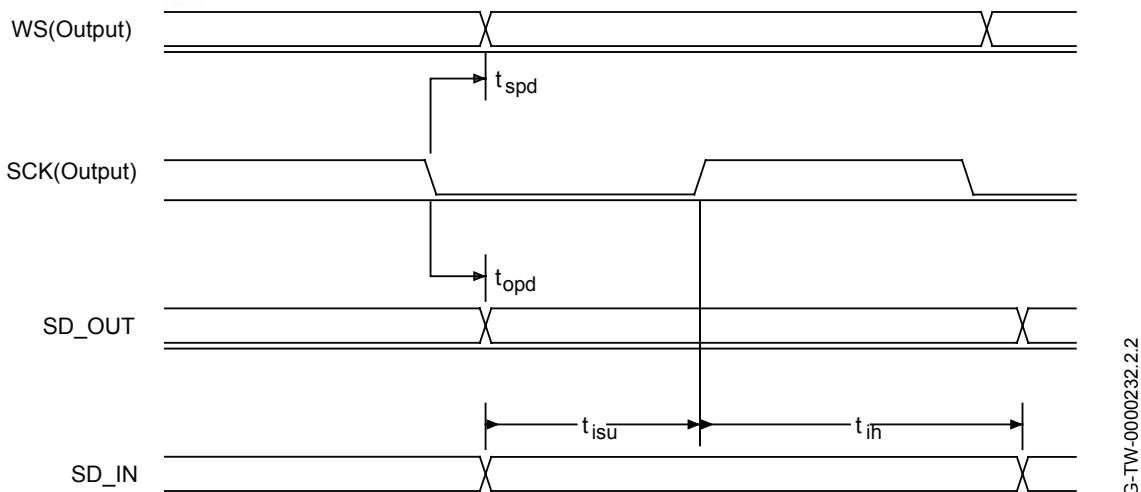
 Table 9.12: I²S Master Mode Timing Parameters, WS and SCK as Outputs


Figure 9.22: Digital Audio Interface Master Timing

10 Power Control and Regulation

For greater power efficiency the CSR8645 BGA contains 2 switch-mode regulators:

- 1 generates a 1.80V supply rail with an output current of 185mA, see Section 10.1.
- 1 generates a 1.35V supply rail with an output current of 160mA, see Section 10.2.
- Combining the 2 switch-mode regulators in parallel generates a single 1.80V supply rail with an output current of 340mA, see Section 10.3.

CSR8645 BGA contains 4 LDO linear regulators:

- 3.30V bypass regulator, see Section 10.4.
- 0.80V to 1.20V VDD_DIG linear regulator, see Section 10.5.
- 1.35V VDD_AUX linear regulator, see Section 10.6.
- 1.35V VDD_ANA linear regulator, see Section 10.7.

The recommended configurations for power control and regulation on the CSR8645 BGA are:

- 3 switch-mode configurations:
 - A 1.80V and 1.35V dual-supply rail system using the 1.80V and 1.35V switch-mode regulators, see Figure 10.1. This is the default power control and regulation configuration for the CSR8645 BGA.
 - A 1.80V single-supply rail system using the 1.80V switch-mode regulator.
 - A 1.80V parallel-supply rail system for higher currents using the 1.80V and 1.35V switch-mode regulators with combined outputs, see Figure 10.2.
- A linear configuration using an external 1.8V rail omitting all regulators

Table 10.1 shows settings for the recommended configurations for power control and regulation on the CSR8645 BGA.

| Supply Configuration | Regulators | | | | Supply Rail | |
|----------------------|-------------|-------|--------------------------|--------------------------|-------------|-------|
| | Switch-mode | | VDD_AUX Linear Regulator | VDD_ANA Linear Regulator | | |
| | 1.8V | 1.35V | | | 1.8V | 1.35V |
| Dual-supply SMPS | ON | ON | OFF | OFF | SMPS | SMPS |
| Single-supply SMPS | ON | OFF | ON | ON | SMPS | LDO |
| Parallel-supply SMPS | ON | ON | ON | ON | SMPS | LDO |
| Linear supply | OFF | OFF | ON | ON | External | LDO |

Table 10.1: Recommended Configurations for Power Control and Regulation

For more information on CSR8645 BGA power supply configuration see the *Configuring the Power Supplies on CSR8670* application note.

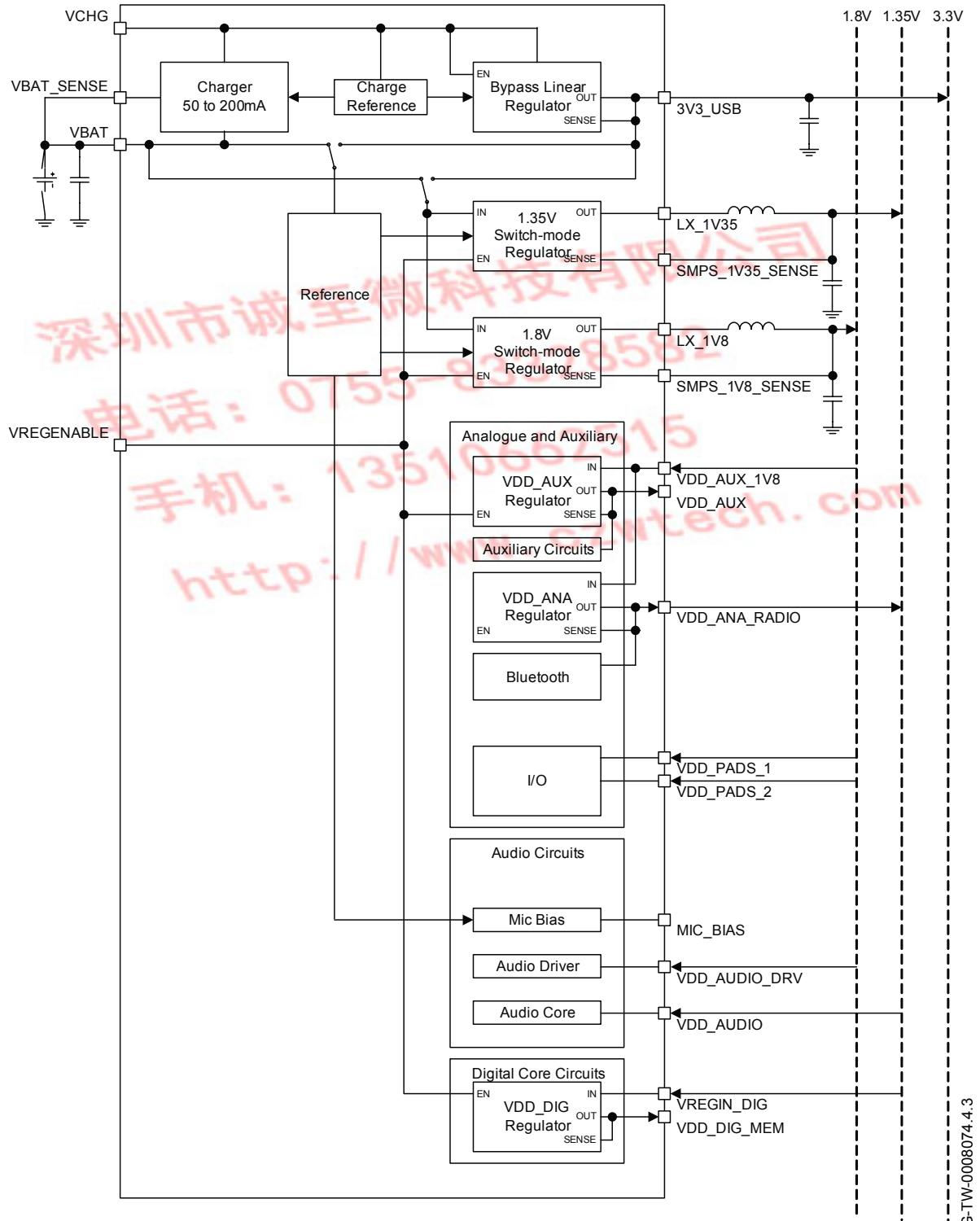
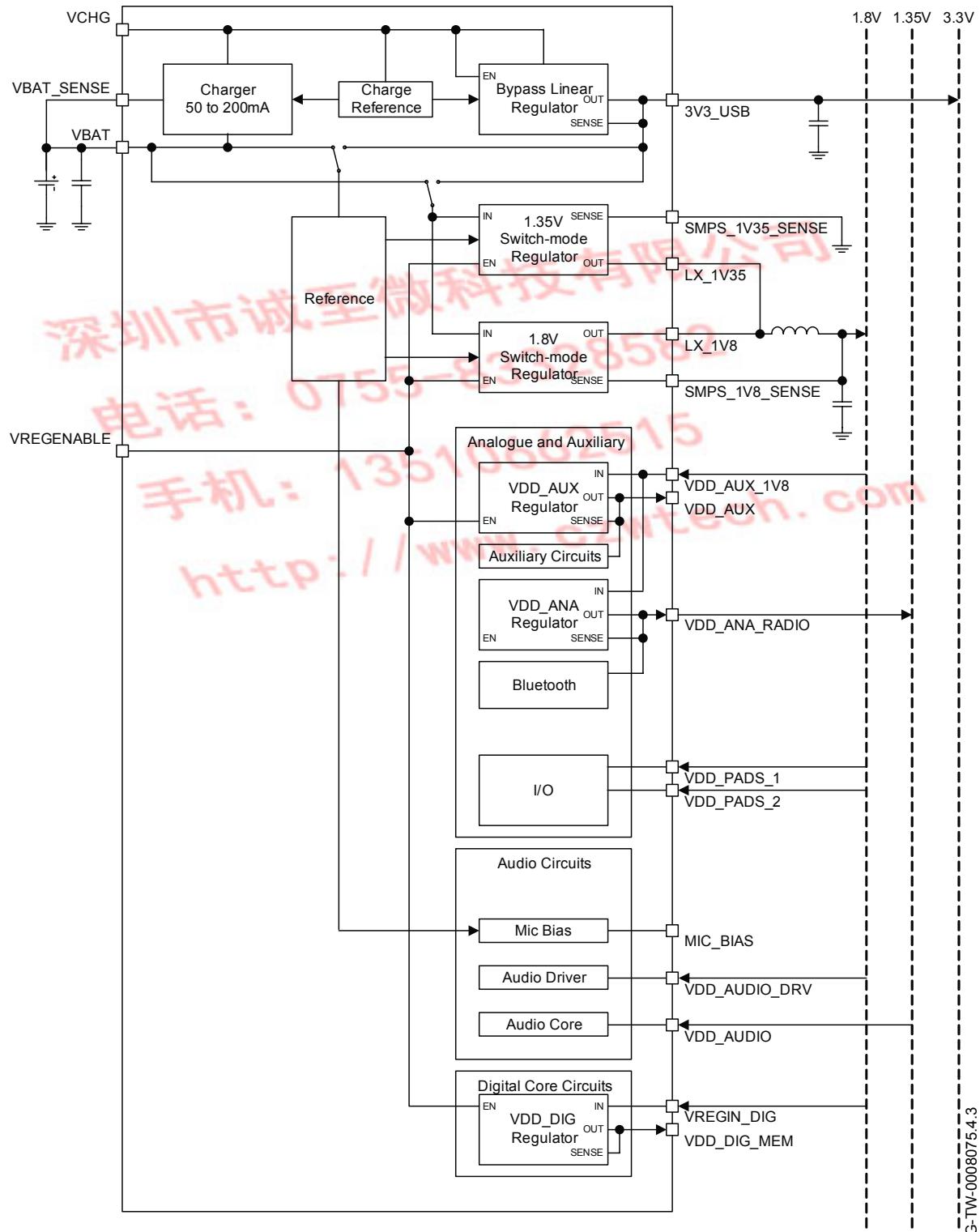


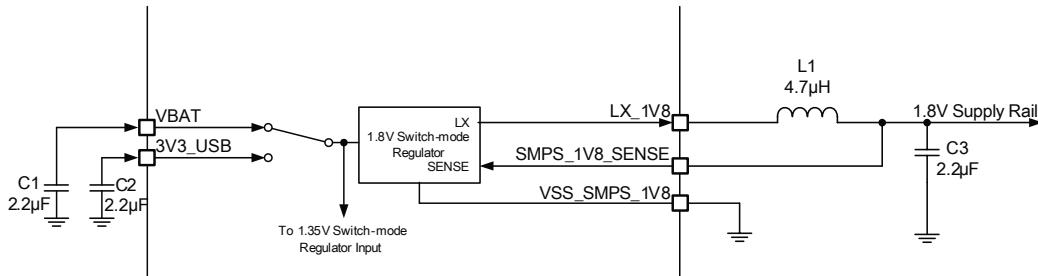
Figure 10.1: 1.80V and 1.35V Dual-supply Switch-mode System Configuration



10.1 1.8V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.80V supply rail.

Figure 10.3 shows that an external LC filter circuit of a low-resistance series inductor, L1 (4.7 μ H), followed by a low ESR shunt capacitor, C3 (2.2 μ F), is required between the LX_1V8 terminal and the 1.80V supply rail. Connect the 1.80V supply rail and the VDD_AUX_1V8 pin.



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Figure 10.3: 1.8V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, VBAT and 3V3_USB, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V8.

Also minimise the collective parasitic capacitance on the track between LX_1V8 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 14.3.1.1 requires a total resistance of <1.0 Ω (<0.5 Ω recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80V supply rail.

The following enable the 1.80V switch-mode regulator:

- VREGENABLE pin
- The CSR8645 BGA firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.35V switch-mode regulator.

When the 1.80V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and 3V3_USB
- The regulator output LX_1V8

10.2 1.35V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.35V supply rail.

Figure 10.4 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7 μ H), followed by a low ESR shunt capacitor, C3 (4.7 μ F), is required between the LX_1V35 terminal and the 1.35V supply rail. Connect the 1.35V supply rail and the SMPS_1V35_SENSE pin.

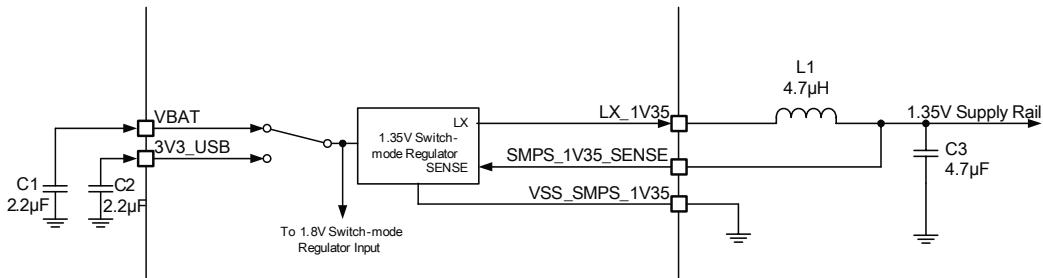


Figure 10.4: 1.35V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, VBAT and 3V3_USB, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 14.3.2.1 requires a total resistance of $<1.0\Omega$ ($<0.5\Omega$ recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.35V supply rail.

The following enable the 1.35V switch-mode regulator:

- VREGENABLE pin
- The CSR8645 BGA firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.80V switch-mode regulator.

When the 1.35V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and 3V3_USB
- The regulator output LX_1V35

10.3 1.8V and 1.35V Switch-mode Regulators Combined

For applications that require a single 1.80V supply rail with higher currents CSR recommends combining the outputs of the integrated 1.80V and 1.35V switch-mode regulators in parallel to power a single 1.80V supply rail, see Figure 10.5.

Figure 10.5 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7µH), followed by a low ESR shunt capacitor, C3 (2.2µF), is required between the LX_1V8 terminal and the 1.80V supply rail. Connect the 1.80V supply rail and the VDD_AUX_1V8 pin and ground the SMPS_1V35_SENSE pin.

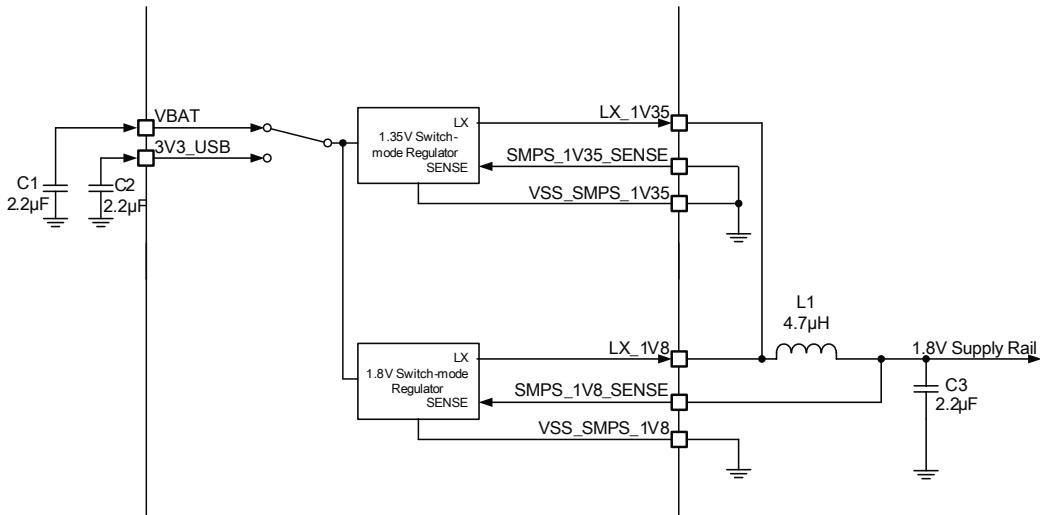


Figure 10.5: 1.8V and 1.35V Switch-mode Regulators Outputs Parallel Configuration

Minimise the series resistance of the tracks between the regulator input VBAT and 3V3_USB, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3, VSS_SMPS_1V8 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V8, LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 14.3.1.2 requires a total resistance of $<1.0\Omega$ ($<0.5\Omega$ recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8, LX_1V35 and the inductor.
- The inductor L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80V supply rail.

The following enable the 1.80V switch-mode regulator:

- VREGENABLE pin
- The CSR8645 BGA firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET.

When the 1.80V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and 3V3_USB
- The regulator output LX_1V8

10.4 Bypass LDO Linear Regulator

The integrated bypass LDO linear regulator is available as a 3.30V supply rail and is an alternative supply rail to the battery supply. This is especially useful when the battery has no charge and the CSR8645 BGA needs to power up. The input voltage should be between 4.75 / 3.10V and 5.25V.

Note:

The integrated bypass LDO linear regulator can operate down to 3.0V with a reduced performance.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 2.2 μ F to the 3V3_USB pin.

The output voltage is switched on when VCHG gets above 3.0V.

10.5 Low-voltage VDD_DIG Linear Regulator

The integrated low-voltage VDD_DIG linear regulator powers the digital circuits on CSR8645 BGA. Externally decouple the output of this regulator using a low ESR MLC capacitor of 470nF.

10.6 Low-voltage VDD_AUX Linear Regulator

The integrated low-voltage VDD_AUX linear regulator is optionally available to provide a 1.35V auxiliary supply rail when the 1.35V switch-mode regulator is not used. When using the integrated low-voltage VDD_AUX linear regulator, externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 470nF to the VDD_AUX pin.

10.7 Low-voltage VDD_ANA Linear Regulator

The integrated low-voltage VDD_ANA linear regulator is optionally available to power the 1.35V analogue supply rail when the 1.35V switch-mode regulator is not used. When using the integrated low-voltage VDD_ANA linear regulator, externally decouple the output of this regulator using a 2.2 μ F low ESR MLC capacitor to the VDD_ANA_RADIO pin.

10.8 Voltage Regulator Enable

When using the integrated regulators the voltage regulator enable pin, VREGENABLE, enables the CSR8645 BGA and the following regulators:

- 1.8V switch-mode regulator
- 1.35V switch-mode regulator
- Low-voltage VDD_DIG linear regulator
- Low-voltage VDD_AUX linear regulator

The VREGENABLE pin is active high, with a weak pull-down.

CSR8645 BGA boots-up when the voltage regulator enable pin is pulled high, enabling the regulators. The firmware then latches the regulators on. The voltage regulator enable pin can then be released.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

Note:

VREGENABLE should be asserted after the VBAT supply when VREGENABLE is not used as a power-on button.

10.9 External Regulators and Power Sequencing

CSR recommends that the integrated regulators supply the CSR8645 BGA and it is configured based on the information in this data sheet.

If any of the supply rails for the CSR8645 BGA are supplied from an external regulator, then it should match or be better than the internal regulator available on CSR8645 BGA. For more information see regulator characteristics in Section 14.

Note:

The internal regulators described in Section 10.1 to Section 10.7 are not recommended for external circuitry other than that shown in Section 12.

For information about power sequencing of external regulators to supply the CSR8645 BGA contact CSR.

10.10 Reset, RST#

CSR8645 BGA is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. CSR recommends applying RST# for a period >5ms.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

10.10.1 Digital Pin States on Reset

Table 10.2 shows the pin states of CSR8645 BGA on reset.

| Pin Name | I/O Type | Full Chip Reset | Pin Name | I/O Type | Full Chip Reset |
|----------|-----------------------|-----------------|----------|-----------------------|-----------------|
| USB_DP | Digital bidirectional | N/A | PIO[10] | Digital bidirectional | PDS |
| USB_DN | Digital bidirectional | N/A | PIO[11] | Digital bidirectional | PDS |
| PIO[0] | Digital bidirectional | PUS | PIO[12] | Digital bidirectional | PUS |
| PIO[1] | Digital bidirectional | PUS | PIO[13] | Digital bidirectional | PDS |
| PIO[2] | Digital bidirectional | PDW | PIO[14] | Digital bidirectional | PUS |
| PIO[3] | Digital bidirectional | PDW | PIO[15] | Digital bidirectional | PUS |
| PIO[4] | Digital bidirectional | PDW | PIO[16] | Digital bidirectional | PUS |
| PIO[5] | Digital bidirectional | PDW | PIO[17] | Digital bidirectional | PDS |
| PIO[6] | Digital bidirectional | PDS | PIO[18] | Digital bidirectional | PDW |
| PIO[7] | Digital bidirectional | PDS | PIO[19] | Digital bidirectional | PDW |
| PIO[8] | Digital bidirectional | PUS | PIO[20] | Digital bidirectional | PDW |
| PIO[9] | Digital bidirectional | PDS | PIO[21] | Digital bidirectional | PDW |

Table 10.2: Pin States on Reset

Note:

PUS = Strong pull-up

PDS = Strong pull-down

PUW = Weak pull-up

PDW = Weak pull-down

10.10.2 Status After Reset

The status of CSR8645 BGA after a reset is:

- Warm reset: baud rate and RAM data remain available
- Cold reset: baud rate and RAM data not available

10.11 Automatic Reset Protection

CSR8645 BGA includes an automatic reset protection circuit which restarts/resets CSR8645 BGA when an unexpected reset occurs, e.g. ESD strike or lowering of RST#. The automatic reset protection circuit enables resets from the VM without the requirement for external circuitry.

Note:

The reset protection is cleared after typically 2s (1.6s min to 2.4s max).

If RST# is held low for >2.4s CSR8645 BGA turns off. A rising edge on VREGENABLE or VCHG is required to power on CSR8645 BGA.

11 Battery Charger

11.1 Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the VM, see Section 11.3. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see Table 11.1 and Figure 11.1.

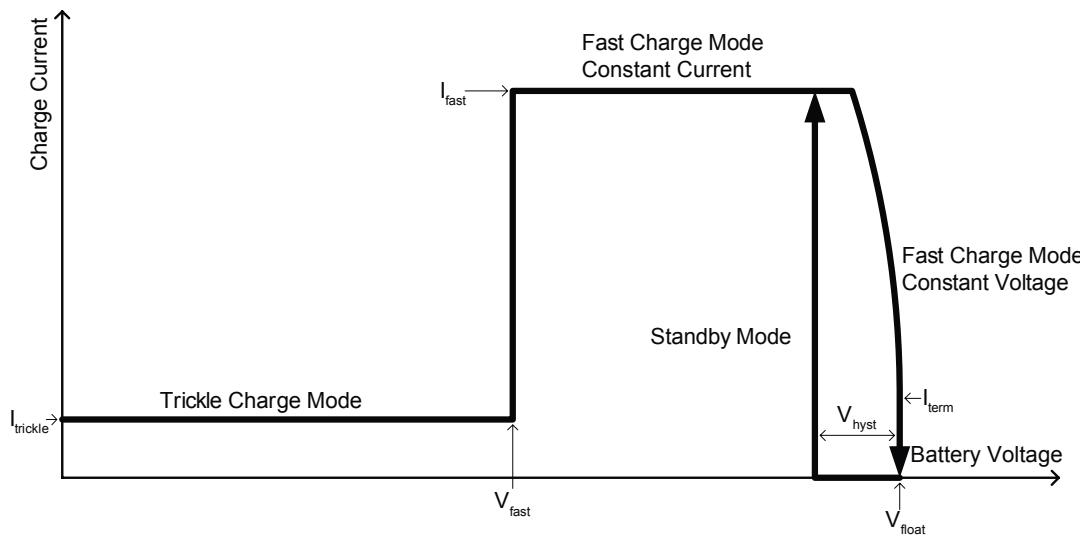
The internal charger circuit can provide up to 200mA of charge current, for currents higher than this the CSR8645 BGA can control an external pass transistor, see Section 11.5.

| Mode | Battery Charger Enabled | VBAT_SENSE |
|----------------|-------------------------|---|
| Disabled | No | X |
| Trickle charge | Yes | >0 and $<V_{fast}$ |
| Fast charge | Yes | $>V_{fast}$ and $<V_{float}$ |
| Standby | Yes | I_{term} ^(a) and $>(V_{float} - V_{hyst})$ |
| Error | Yes | $>(V_{CHG} - 50mV)$ |

Table 11.1: Battery Charger Operating Modes Determined by Battery Voltage and Current

(a) I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting

Figure 11.1 shows the mode-to-mode transition voltages. These voltages are fixed and calibrated by CSR, see Section 11.2. The transition between modes can occur at any time.



G-TW-0005583.3.2

Figure 11.1: Battery Charger Mode-to-Mode Transition Diagram

Note:

The battery voltage remains constant in Fast Charge Constant Voltage Mode, the curved line on Figure 11.1 is for clarity only.

11.1.1 Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

11.1.2 Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast} , is sourced from the VBAT pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

11.1.3 Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast} , the current sourced from the VBAT pin increases to I_{fast} . I_{fast} is between 10mA and 200mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float} , then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term} , the charging stops and the charger enters standby mode. I_{term} is typically 10% of the fast charge current.

11.1.4 Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float} , the charger re-enters fast charge mode.

11.1.5 Error Mode

The charger enters the error mode if the voltage on the VCHG pin is too low to operate the charger correctly (VBAT_SENSE is greater than VCHG - 50mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

11.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written by CSR into internal ROM when each IC is characterised. CSR provides various PS Keys for overriding the default trims, see Section 11.4.

11.3 VM Battery Charger Control

The VM charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information
- Driving the user visible charger status LED(s)

11.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and call traps from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

For more information on the CSR8645 BGA, including details on setting up, calibrating, trimming and the PS Keys, see *Lithium Polymer Battery Charger Calibration and Operation for CSR8670* application note.

11.5 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, R_{sense} , connected in series with the external pass device, see Figure 11.2. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across R_{sense} is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

In Figure 11.2, R1 (220m Ω) and C1 (4.7 μ F) form an RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be $<1.0\Omega$.

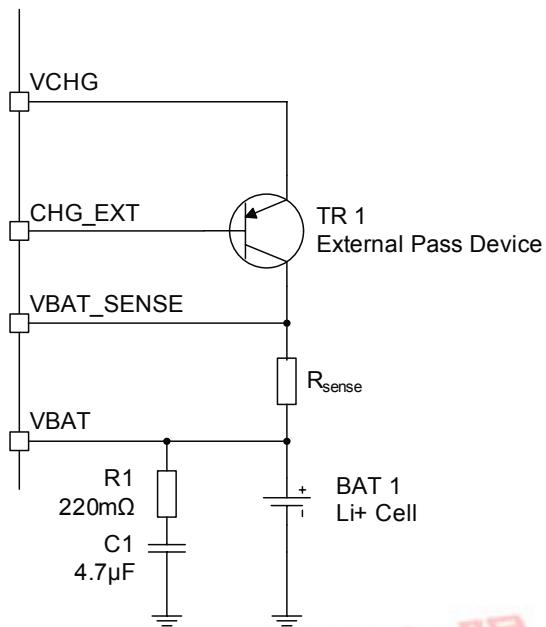
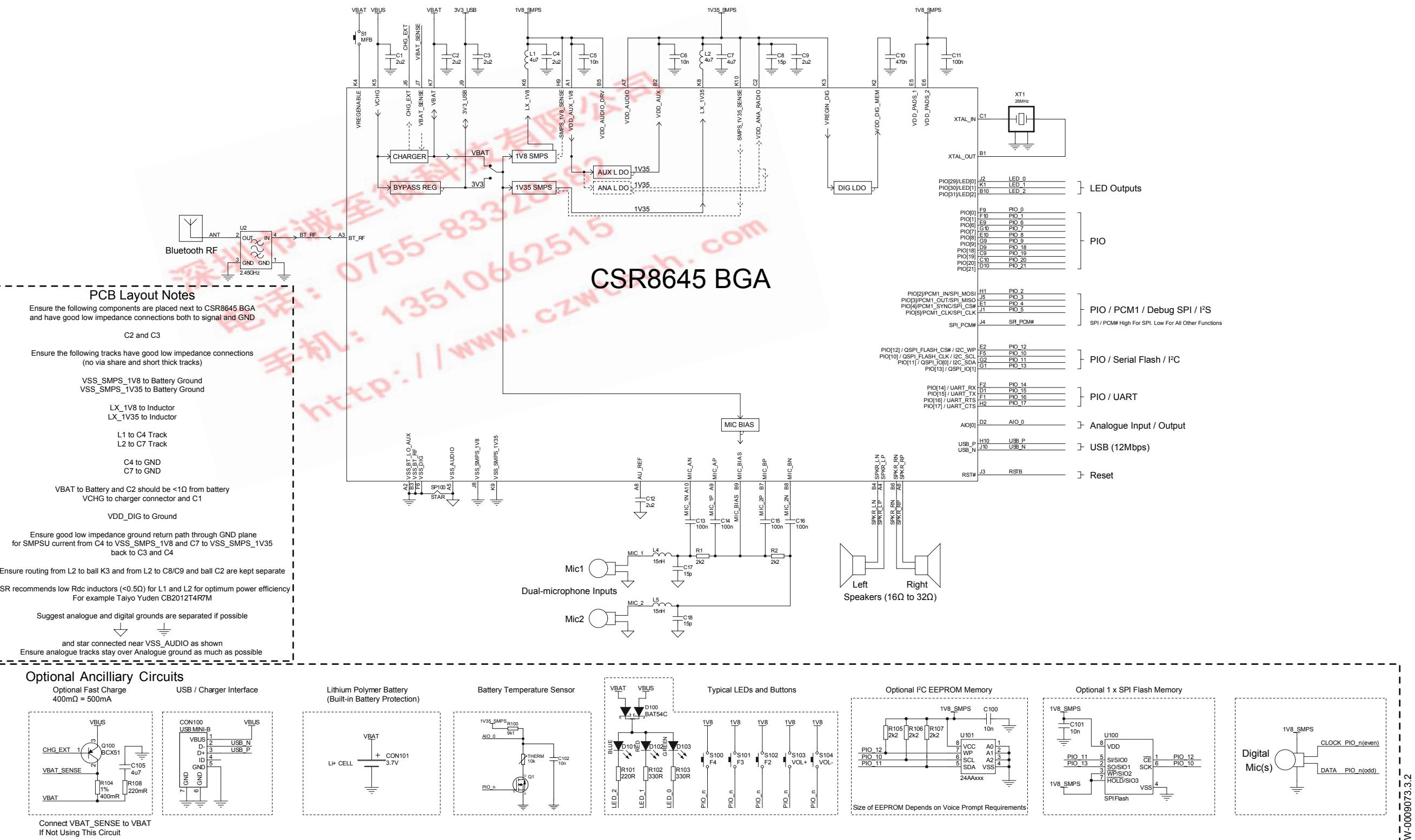


Figure 11.2: Battery Charger External Mode Typical Configuration

G-TW-00055852-3

12 Example Application Schematic



13 Example Application Using Different Power Supply Configurations

Single 1.8V Only Supply. No USB, No Switch-mode

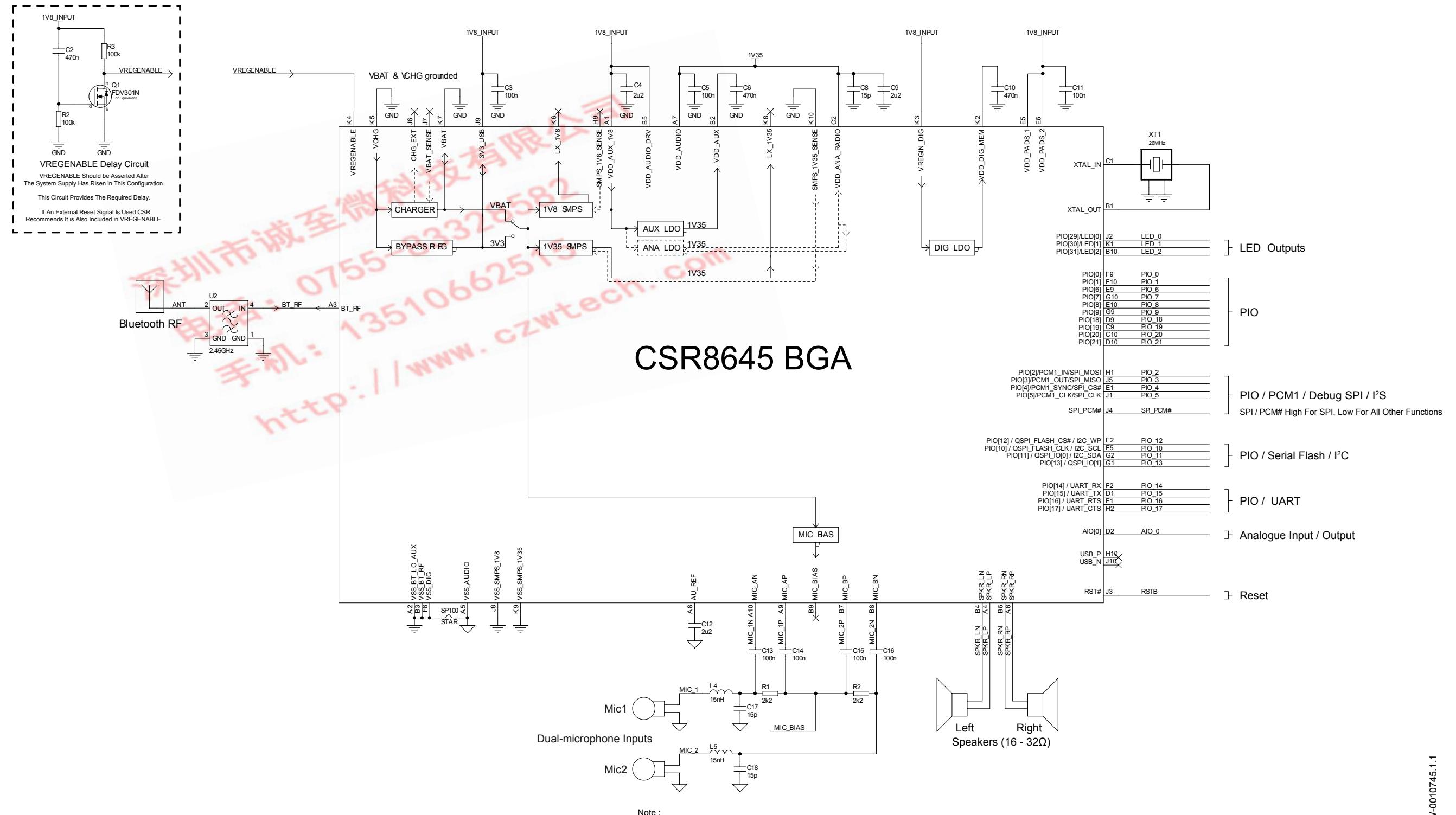


Figure 13.1: External 1.8V Supply Example Application

Single 3.3V Only Supply. USB, Dual Switch-mode.

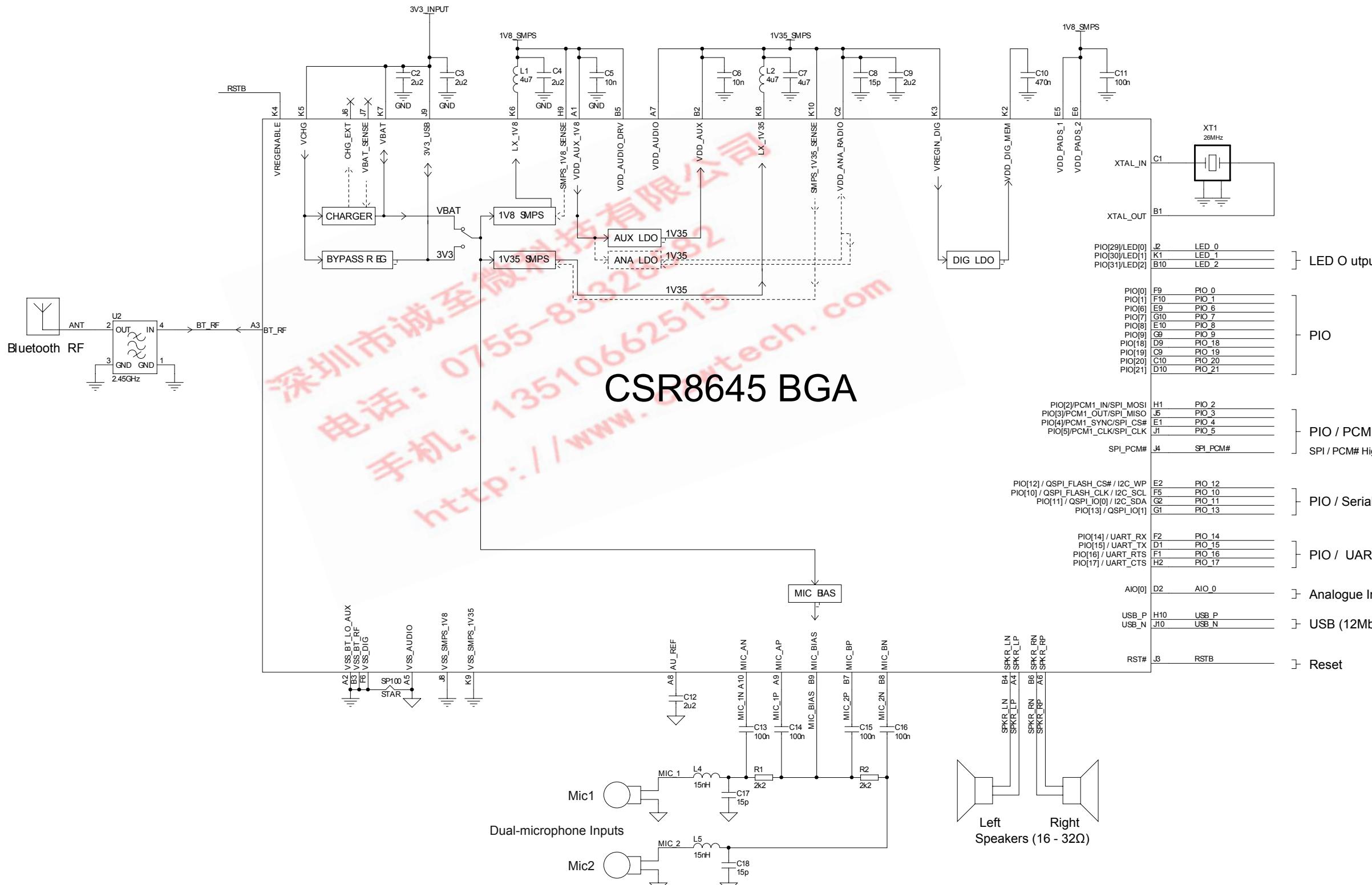


Figure 13.2: External 3.3V Supply Example Application

USB Audio Dongle. Single Ganged, 1.8V Switch-mode.

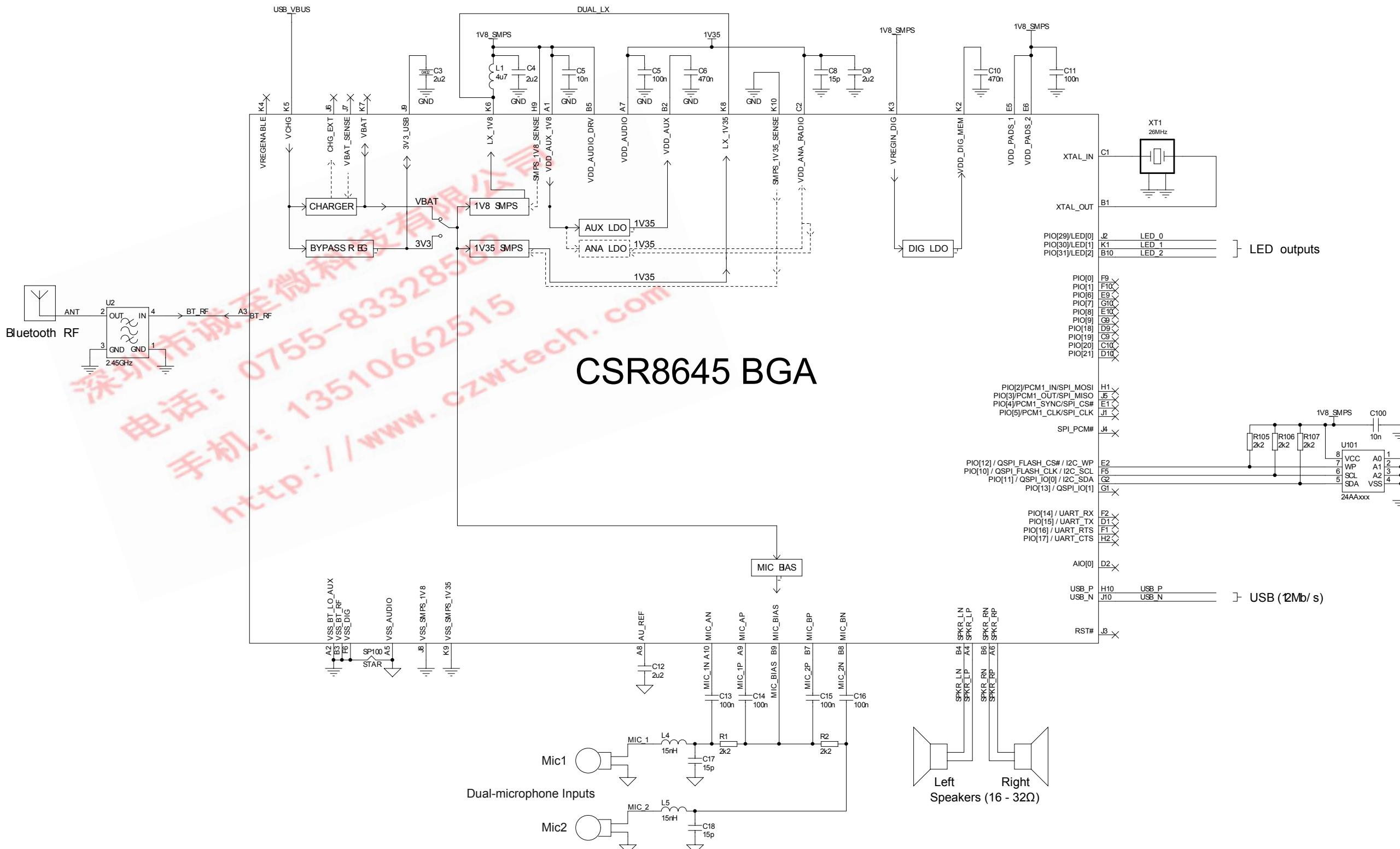


Figure 13.3: USB Audio Dongle Example Application

14 Electrical Characteristics

14.1 Absolute Maximum Ratings

| Rating | | Min | Max | Unit |
|-------------------------|-----------------|-----------|-----------|------|
| Storage temperature | | -40 | 105 | °C |
| Supply Voltage | | | | |
| Charger | VCHG | -0.4 | 5.75 | V |
| LEDs | LED[2:0] | -0.4 | 4.40 | V |
| Battery | VBAT_SENSE | -0.4 | 4.20 | V |
| | VREGENABLE | -0.4 | 4.40 | V |
| 1.8V | VDD_AUDIO_DRV | -0.4 | 1.95 | V |
| | VDD_AUX_1V8 | -0.4 | 1.95 | V |
| | VDD_PADS_1 | -0.4 | 3.60 | V |
| | VDD_PADS_2 | -0.4 | 3.60 | V |
| | VDD_AUX_1V8 | -0.4 | 1.95 | V |
| 1.35V | SMPS_1V35_SENSE | -0.4 | 1.45 | V |
| | VDD_AUDIO | -0.4 | 1.45 | V |
| | VREGIN_DIG | -0.4 | 1.95 | V |
| Other terminal voltages | | VSS - 0.4 | VDD + 0.4 | V |

14.2 Recommended Operating Conditions

| Rating | | Min | Typ | Max | Unit |
|-----------------------------|-----------------|-------------|--------------|------|------|
| Operating temperature range | | -40 | 20 | 85 | °C |
| Supply Voltage | | | | | |
| Charger | VCHG | 4.75 / 3.10 | 5.00 | 5.75 | V |
| LEDs | LED[2:0] | 1.10 | 3.70 | 4.25 | V |
| Battery | VBAT_SENSE | 0 | 3.70 | 4.30 | V |
| | VREGENABLE | 0 | 3.70 | 4.25 | V |
| 1.8V | VDD_AUDIO_DRV | 1.70 | 1.80 | 1.95 | V |
| | VDD_AUX_1V8 | 1.70 | 1.80 | 1.95 | V |
| | VDD_PADS_1 | 1.70 | 1.80 | 3.60 | V |
| | VDD_PADS_2 | 1.70 | 1.80 | 3.60 | V |
| | VDD_AUX_1V8 | 1.25 | 1.80 | 1.95 | V |
| 1.35V | SMPS_1V35_SENSE | 1.30 | 1.35 | 1.40 | V |
| | VDD_AUDIO | 1.30 | 1.35 | 1.40 | V |
| | VREGIN_DIG | 1.30 | 1.35 or 1.80 | 1.95 | V |

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14.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

14.3.1 Regulators: Available For External Use

14.3.1.1 1.8V Switch-mode Regulator

| 1.8V Switch-mode Regulator | Min | Typ | Max | Unit |
|--|-------|------|------|------|
| Input voltage | 2.80 | 3.70 | 4.25 | V |
| Output voltage | 1.70 | 1.80 | 1.90 | V |
| Normal Operation | | | | |
| Transient settling time | - | 30 | - | µs |
| Load current | - | - | 185 | mA |
| Current available for external use, audio with 16Ω load ^(a) | - | - | 25 | mA |
| Peak conversion efficiency ^(b) | - | 90 | - | % |
| Switching frequency | 3.63 | 4.00 | 4.00 | MHz |
| Inductor saturation current, audio and 16Ω load | 250 | - | - | mA |
| Inductor ESR | 0.1 | 0.3 | 0.8 | Ω |
| Low-power Mode, Automatically Entered in Deep Sleep | | | | |
| Transient settling time | - | 200 | - | µs |
| Load current | 0.005 | - | 5 | mA |
| Current available for external use | - | - | 5 | mA |
| Peak conversion efficiency | - | 85 | - | % |
| Switching frequency | 100 | - | 200 | kHz |

(a) More current available for audio loads above 16Ω.

(b) Conversion efficiency depends on inductor selection.

14.3.1.2 Combined 1.8V and 1.35V Switch-mode Regulator

| Combined 1.8V and 1.35V Switch-mode Regulator | Min | Typ | Max | Unit |
|--|-------|------|------|------|
| Input voltage | 2.80 | 3.60 | 4.25 | V |
| Output voltage | 1.70 | 1.80 | 1.90 | V |
| Normal Operation | | | | |
| Transient settling time | - | 30 | - | μs |
| Load current | - | - | 340 | mA |
| Current available for external use, audio with 16Ω load ^(a) | - | - | 25 | mA |
| Peak conversion efficiency ^(b) | - | 90 | - | % |
| Switching frequency | 3.63 | 4.00 | 4.00 | MHz |
| Inductor saturation current, audio and 16Ω load | 400 | - | - | mA |
| Inductor ESR | 0.1 | 0.3 | 0.8 | Ω |
| Low-power Mode, Automatically Entered in Deep Sleep | | | | |
| Transient settling time | - | 200 | - | μs |
| Load current | 0.005 | - | 5 | mA |
| Current available for external use | - | - | 5 | mA |
| Peak conversion efficiency | - | 85 | - | % |
| Switching frequency | 100 | - | 200 | kHz |

(a) More current available for audio loads above 16Ω.

(b) Conversion efficiency depends on inductor selection.

14.3.1.3 Bypass LDO Regulator

| Normal Operation | Min | Typ | Max | Unit |
|-------------------------------------|-------------|------|------|------|
| Input voltage ^(a) | 4.75 / 3.10 | 5.00 | 5.25 | V |
| Output voltage ($V_{in} > 4.75V$) | 3.00 | 3.30 | 3.60 | V |
| Output current ($V_{in} > 4.75V$) | - | - | 250 | mA |

(a) Minimum input voltage of 4.75V is required for full specification, regulator operates at reduced load current from 3.1V.

14.3.2 Regulators: For Internal Use Only

14.3.2.1 1.35V Switch-mode Regulator

| 1.35V Switch-mode Regulator | Min | Typ | Max | Unit |
|---|-------|------|------|------|
| Input voltage | 2.80 | 3.60 | 4.25 | V |
| Output voltage | 1.30 | 1.35 | 1.40 | V |
| Normal Operation | | | | |
| Transient settling time | - | 30 | - | μs |
| Load current | - | - | 160 | mA |
| Current available for external use | - | - | 0 | mA |
| Peak conversion efficiency ^(a) | - | 88 | - | % |
| Switching frequency | 3.63 | 4.00 | 4.00 | MHz |
| Inductor saturation current, audio and 16Ω load | 220 | - | - | mA |
| Inductor ESR | 0.1 | 0.3 | 0.8 | Ω |
| Low-power Mode, Automatically Entered in Deep Sleep | | | | |
| Transient settling time | - | 200 | - | μs |
| Load current | 0.005 | - | 5 | mA |
| Current available for external use | - | - | 0 | mA |
| Peak conversion efficiency | - | 85 | - | % |
| Switching frequency | 100 | - | 200 | kHz |

(a) Conversion efficiency depends on inductor selection.

14.3.2.2 Low-voltage VDD_DIG Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|-------------------------------|------|--------------|------|------|
| Input voltage | 1.30 | 1.35 or 1.80 | 1.95 | V |
| Output voltage ^(a) | 0.80 | 0.90 / 1.20 | 1.25 | V |
| Internal load current | - | - | 80 | mA |

^(a) Output voltage level is software controlled

14.3.2.3 Low-voltage VDD_AUX Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|-----------------------|------|------|------|------|
| Input voltage | 1.70 | 1.80 | 1.95 | V |
| Output voltage | 1.30 | 1.35 | 1.45 | V |
| Internal load current | - | - | 5 | mA |

14.3.2.4 Low-voltage VDD_ANA Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|------------------|------|------|------|------|
| Input voltage | 1.70 | 1.80 | 1.95 | V |
| Output voltage | 1.30 | 1.35 | 1.45 | V |
| Load current | - | - | 60 | mA |

14.3.3 Regulator Enable

| VREGENABLE, Switching Threshold | Min | Typ | Max | Unit |
|---------------------------------|-----|-----|-----|------|
| Rising threshold | 1.0 | - | - | V |

14.3.4 Battery Charger

| Battery Charger | Min | Typ | Max | Unit |
|------------------------------------|-------------|------|------|------|
| Input voltage, VCHG ^(a) | 4.75 / 3.10 | 5.00 | 5.75 | V |

^(a) Reduced specification from 3.1V to 4.75V. Full specification >4.75V.

| Trickle Charge Mode | | Min | Typ | Max | Unit |
|---|--|-----|-----|-----|------|
| Charge current $I_{trickle}$, as percentage of fast charge current | | 8 | 10 | 12 | % |
| V_{fast} rising threshold | | - | 2.9 | - | V |
| V_{fast} rising threshold trim step size | | - | 0.1 | - | V |
| V_{fast} falling threshold | | - | 2.8 | - | V |

| Fast Charge Mode | | Min | Typ | Max | Unit |
|---|--|------|------|------|------|
| Charge current during constant current mode, I_{fast} | Maximum charge setting ($V_{CHG}-V_{BAT} > 0.55V$) | 194 | 200 | 206 | mA |
| | Minimum charge setting ($V_{CHG}-V_{BAT} > 0.55V$) | - | 10 | - | mA |
| Reduced headroom charge current, as a percentage of I_{fast} | ($V_{CHG}-V_{BAT} < 0.55V$) | 50 | - | 100 | % |
| Charge current step size | | - | 10 | - | mA |
| V_{float} threshold, calibrated | | 4.16 | 4.20 | 4.24 | V |
| Charge termination current I_{term} , as percentage of I_{fast} | | 7 | 10 | 20 | % |

| Standby Mode | | Min | Typ | Max | Unit |
|--|--|-----|-----|-----|------|
| Voltage hysteresis on V_{BAT} , V_{hyst} | | 100 | - | 150 | mV |

| Error Charge Mode | | Min | Typ | Max | Unit |
|---|--|-----|-----|-----|------|
| Headroom ^(a) error falling threshold | | - | 50 | - | mV |

^(a) Headroom = $V_{CHG} - V_{BAT}$

| External Charge Mode ^(a) | Min | Typ | Max | Unit |
|---|-----|-----|------|------|
| Fast charge current, I_{fast} | 200 | - | 500 | mA |
| Control current into CHG_EXT | 0 | - | 20 | mA |
| Voltage on CHG_EXT | 0 | - | 5.75 | V |
| External pass device h_{fe} | - | 50 | - | - |
| Sense voltage, between VBAT_SENSE and VBAT at maximum current | 195 | 200 | 205 | mV |

(a) In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

14.3.5 USB

| | Min | Typ | Max | Unit |
|--|---------------|-----|---------------|------|
| 3V3_USB for correct USB operation | 3.1 | 3.3 | 3.6 | V |
| Input Threshold | | | | |
| V_{IL} input logic level low | - | - | 0.3 x 3V3_USB | V |
| V_{IH} input logic level high | 0.7 x 3V3_USB | - | - | V |
| Output Voltage Levels to Correctly Terminated USB Cable | | | | |
| V_{OL} output logic level low | 0 | - | 0.2 | V |
| V_{OH} output logic level high | 2.8 | - | 3V3_USB | V |

14.3.6 Clocks

| Crystal Oscillator | Min | Typ | Max | Unit |
|--------------------------|-----|-----|-----|------|
| Frequency | 16 | 26 | 32 | MHz |
| Crystal load capacitance | - | 9 | - | pF |
| Frequency stability | - | - | 20 | ppm |
| Frequency tolerance | - | - | ±20 | ppm |
| Transconductance | 2 | - | - | mS |

14.3.7 Stereo Codec: Analogue to Digital Converter

| Analogue to Digital Converter | | | | | | |
|--|--|---------------------|-----|--------|------|------|
| Parameter | Conditions | | Min | Typ | Max | Unit |
| Resolution | - | | - | - | 16 | Bits |
| Input Sample Rate, F_{sample} | - | | 8 | - | 48 | kHz |
| SNR | $f_{\text{in}} = 1\text{kHz}$ $B/W = 20\text{Hz} \rightarrow F_{\text{sample}}/2$ (20kHz max) A-Weighted $\text{THD+N} < 0.1\%$ 1.6V _{pk-pk} input | F_{sample} | | | | |
| | | 8kHz | - | 93.5 | - | dB |
| | | 16kHz | - | 92.5 | - | dB |
| | | 32kHz | - | 91.4 | - | dB |
| | | 44.1kHz | - | 90.4 | - | dB |
| | | 48kHz | - | 89.6 | - | dB |
| THD+N | $f_{\text{in}} = 1\text{kHz}$ $B/W = 20\text{Hz} \rightarrow F_{\text{sample}}/2$ (20kHz max) 1.6V _{pk-pk} input | F_{sample} | | | | |
| | | 8kHz | - | 0.0041 | - | % |
| | | 48kHz | - | 0.0072 | - | % |
| Digital gain | Digital gain resolution = 1/32 | | -24 | - | 21.5 | dB |
| Analogue gain | Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analogue setting = -3dB to 12dB in 3dB steps | | -3 | - | 42 | dB |
| Stereo separation (crosstalk) | | | - | -88.5 | - | dB |

14.3.8 Stereo Codec: Digital to Analogue Converter

| Digital to Analogue Converter | | | | | | |
|---|--|---------------------|-------|-------|--------|------|
| Parameter | Conditions | | Min | Typ | Max | Unit |
| Resolution | - | | - | - | 16 | Bits |
| Output Sample Rate, F_{sample} | - | | 8 | - | 96 | kHz |
| SNR | $f_{\text{in}} = 1\text{kHz}$ B/W = 20Hz→20kHz A-Weighted THD+N < 0.1% 0dBFS input | F_{sample} | Load | | | |
| | | 48kHz | 100kΩ | - | 95.6 | - |
| | | 48kHz | 32Ω | - | 95.8 | - |
| | | 48kHz | 16Ω | - | 95.6 | - |
| THD+N | $f_{\text{in}} = 1\text{kHz}$ B/W = 20Hz→20kHz 0dBFS input | F_{sample} | Load | | | |
| | | 8kHz | 100kΩ | - | 0.0025 | - |
| | | 8kHz | 32Ω | - | 0.0056 | - |
| | | 8kHz | 16Ω | - | 0.0108 | - |
| | | 48kHz | 100kΩ | - | 0.0027 | - |
| | | 48kHz | 32Ω | - | 0.0067 | - |
| | | 48kHz | 16Ω | - | 0.0122 | - |
| Digital Gain | Digital Gain Resolution = 1/32 | | -24 | - | 21.5 | dB |
| Analogue Gain | Analogue Gain Resolution = 3dB | | -21 | - | 0 | dB |
| Stereo separation (crosstalk) | | | - | -87.5 | - | dB |

14.3.9 Digital

| Digital Terminals | Min | Typ | Max | Unit |
|--|-------------------|------|-------------|---------------|
| Input Voltage | | | | |
| V_{IL} input logic level low | -0.4 | - | 0.4 | V |
| V_{IH} input logic level high | $0.7 \times VDD$ | - | $VDD + 0.4$ | V |
| Tr/Tf | - | - | 25 | ns |
| Output Voltage | | | | |
| V_{OL} output logic level low, $I_{OL} = 4.0\text{mA}$ | - | - | 0.4 | V |
| V_{OH} output logic level high, $I_{OH} = -4.0\text{mA}$ | $0.75 \times VDD$ | - | - | V |
| Tr/Tf | - | - | 5 | ns |
| Input and Tristate Currents | | | | |
| Strong pull-up | -150 | -40 | -10 | μA |
| Strong pull-down | 10 | 40 | 150 | μA |
| Weak pull-up | -5 | -1.0 | -0.33 | μA |
| Weak pull-down | 0.33 | 1.0 | 5.0 | μA |
| C_I Input Capacitance | 1.0 | - | 5.0 | pF |

14.3.10 LED Driver Pads

| LED Driver Pads | | Min | Typ | Max | Unit |
|---|----------------------|-----|-----|------|----------|
| Current, I_{PAD} | High impedance state | - | - | 5 | μA |
| | Current sink state | - | - | 10 | mA |
| LED pad voltage, V_{PAD} | $I_{PAD} = 10mA$ | - | - | 0.55 | V |
| LED pad resistance | $V_{PAD} < 0.5V$ | - | - | 40 | Ω |
| V_{OL} output logic level low ^(a) | | - | 0 | - | V |
| V_{OH} output logic level high ^(a) | | - | 0.8 | - | V |
| V_{IL} input logic level low | | - | 0 | - | V |
| V_{IH} input logic level high | | - | 0.8 | - | V |

(a) LED output port is open-drain and requires a pull-up

14.3.11 Auxiliary ADC

| Auxiliary ADC | | Min | Typ | Max | Unit |
|------------------------------------|-----|------|------|---------|-----------|
| Resolution | | - | - | 10 | Bits |
| Input voltage range ^(a) | | 0 | - | VDD_AUX | V |
| Accuracy (Guaranteed monotonic) | INL | -1 | - | 1 | LSB |
| | DNL | 0 | - | 1 | LSB |
| Offset | | -1 | - | 1 | LSB |
| Gain error | | -0.8 | - | 0.8 | % |
| Input bandwidth | | - | 100 | - | kHz |
| Conversion time | | 1.38 | 1.69 | 2.75 | μs |
| Sample rate ^(b) | | - | - | 700 | Samples/s |

(a) LSB size = VDD_AUX/1023

(b) The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

14.3.12 Auxiliary DAC

| Auxiliary DAC | Min | Typ | Max | Unit |
|------------------------------|-------|------|---------|------|
| Resolution | - | - | 10 | Bits |
| Supply voltage, VDD_AUX | 1.30 | 1.35 | 1.40 | V |
| Output voltage range | 0 | - | VDD_AUX | V |
| Full-scale output voltage | 1.30 | 1.35 | 1.40 | V |
| LSB size | 0 | 1.32 | 2.64 | mV |
| Offset | -1.32 | 0 | 1.32 | mV |
| Integral non-linearity | -1 | 0 | 1 | LSB |
| Settling time ^(a) | - | - | 250 | ns |

(a) The settling time does not include any capacitive load

14.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 14.1 shows the ESD handling maximum ratings.

| Condition | Class | Max Rating |
|--|-------|--|
| Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001 | 2 | 2kV (all pins except CHG_EXT; CHG_EXT is rated at 1kV) |
| Machine Model Contact Discharge per JEDEC/EIA JESD22-A115 | 200V | 200V (all pins) |
| Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101 | III | 500V (all pins) |

Table 14.1: ESD Handling Ratings

14.4.1 USB Electrostatic Discharge Immunity

CSR8645 BGA has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

CSR has tested CSR8645 BGA assembled in development kits to assess the Electrostatic Discharge Immunity. The tests were based on IEC 61000-4-2 requirements. Tests were performed up to level 4 (8kV contact discharge / 15kV air discharge).

CSR can demonstrate normal performance up to level 2 (4kV contact discharge / 4kV air discharge) as per IEC 61000-4-2 classification 1. Above level 2, temporary degradation is seen (classification 2).

CSR8645 BGA contains a reset protection circuit and software, which will attempt to re-make any connections lost in a ESD event. If the device at the far end permits this, self-recovery of the Bluetooth link is possible if CSR8645 BGA resets on an ESD strike. This classes CSR8645 BGA as IEC 61000-4-2 classification 2 to level 4 (8kV contact discharge / 15kV air discharge). If self-recovery is not implemented, CSR8645 BGA is IEC 61000-4-2 classification 3 to level 4.

Note:

Any test detailed in the IEC-61000-4-2 level 4 test specification does not damage CSR8645 BGA.

The CSR8645 BGA USB VBUS pin is protected to level 4 using an external 2.2 μ F decoupling capacitor on VCHG.

Important Note:

CSR recommends correct PCB routing and to route the VBUS track through a decoupling capacitor pad.

When the USB connector is a long way from CSR8645 BGA, place an extra 1 μ F or 2.2 μ F capacitor near the USB connector.

No components (including 22 Ω series resistors) are required between CSR8645 BGA and the USB_DP and USB_DN lines.

To recover from an unintended reset, e.g. a large ESD strike, the watchdog and reset protection feature can restart CSR8645 BGA and signal the unintended reset to the VM.

Table 14.2 summarises the level of protection.

| IEC 61000-4-2 Level | ESD Test Voltage (Positive and Negative) | IEC 61000-4-2 Classification | Comments |
|---------------------|--|------------------------------|---|
| 1 | 2kV contact / 2kV air | Class 1 | Normal performance within specification limits |
| 2 | 4kV contact / 4kV air | Class 1 | Normal performance within specification limits |
| 3 | 6kV contact / 8kV air | Class 2 or class 3 | Temporary degradation or operator intervention required |
| 4 | 8kV contact / 15kV air | Class 2 or class 3 | Temporary degradation or operator intervention required |

Table 14.2: USB Electrostatic Discharge Protection Level

For more information contact CSR.

深圳市诚至微科技有限公司
电话：0755-83328582
手机：13510662515
<http://www.czwttech.com>

15 Power Consumption

| DUT Role | Connection | | Packet Type | Packet Size | Average Current | Unit |
|----------|--|---|-------------|-------------|-----------------|------|
| Slave | SCO | | HV3 | 30 | 11.0 | mA |
| Slave | eSCO | | EV3 | 30 | 11.8 | mA |
| Slave | eSCO | | 2EV3 | 60 | 9.2 | mA |
| Slave | SCO | 2-mic CVC: <ul style="list-style-type: none">■ 8kHz sampling■ Narrowband | HV3 | 30 | 12.6 | mA |
| Slave | eSCO | 2-mic CVC: <ul style="list-style-type: none">■ 8kHz sampling■ Narrowband | 2EV3 | 60 | 10.8 | mA |
| Slave | eSCO | 2-mic CVC: <ul style="list-style-type: none">■ 16kHz sampling■ Wideband | 2EV3 | 60 | 11.4 | mA |
| Slave | eSCO | 2-mic CVC: <ul style="list-style-type: none">■ 16kHz sampling■ FESI | 2EV3 | 60 | 10.9 | mA |
| Slave | Stereo high quality SBC: <ul style="list-style-type: none">■ Joint stereo■ Bit-Pool = 50, 16 blocks and 8 sub-bands■ 48kHz sampling■ No sniff■ White noise | | - | - | 13.3 | mA |
| Slave | Stereo low quality SBC: <ul style="list-style-type: none">■ Joint stereo■ Bit-Pool = 20, 16 blocks and 8 sub-bands■ 48kHz sampling■ No sniff■ White noise | | - | - | 11.8 | mA |
| Slave | Stereo high quality MP3: <ul style="list-style-type: none">■ 192kbps■ 48kHz sampling■ No sniff■ White noise | | - | - | 12.5 | mA |

| DUT Role | Connection | | Packet Type | Packet Size | Average Current | Unit |
|----------|--|---|-------------|-------------|-----------------|------|
| Slave | Stereo low quality MP3: ■ 96kbps ■ 48kHz sampling ■ No sniff ■ White noise | | - | - | 11.8 | mA |
| Slave | ACL | Sniff = 500ms | - | - | 213 | µA |
| Slave | ACL | Sniff = 1280ms | - | - | 142 | µA |
| Master | SCO | | HV3 | 30 | 10.8 | mA |
| Master | eSCO | | EV3 | 30 | 11.2 | mA |
| Master | eSCO | | 2EV3 | 60 | 8.8 | mA |
| Master | SCO | 2-mic CVC: ■ 8kHz sampling ■ Narrowband | HV3 | 30 | 12.5 | mA |
| Master | eSCO | 2-mic CVC: ■ 8kHz sampling ■ Narrowband | 2EV3 | 60 | 10.5 | mA |
| Master | eSCO | 2-mic CVC: ■ 16kHz sampling ■ Wideband | 2EV3 | 60 | 11.0 | mA |
| Master | eSCO | 2-mic CVC: ■ 16kHz sampling ■ FESI | 2EV3 | 60 | 10.6 | mA |

| DUT Role | Connection | | Packet Type | Packet Size | Average Current | Unit |
|----------|---|----------------|-------------|-------------|-----------------|------|
| Master | Stereo high quality SBC: ▪ Joint stereo ▪ Bit-Pool = 50, 16 blocks and 8 sub-bands ▪ 48kHz sampling ▪ No sniff ▪ White noise | | - | - | 13.2 | mA |
| Master | Stereo low quality SBC: ▪ Joint stereo ▪ Bit-Pool = 20, 16 blocks and 8 sub-bands ▪ 48kHz sampling ▪ No sniff ▪ White noise | | - | - | 10.9 | mA |
| Master | Stereo high quality MP3: ▪ 192kbps ▪ 48kHz sampling ▪ No sniff ▪ White noise | | - | - | 11.8 | mA |
| Master | Stereo low quality MP3: ▪ 96kbps ▪ 48kHz sampling ▪ No sniff ▪ White noise | | - | - | 10.8 | mA |
| Master | ACL | Sniff = 500ms | - | - | 197 | µA |
| Master | ACL | Sniff = 1280ms | - | - | 142 | µA |

Note:

Current consumption values are taken with:

- VBAT pin = 3.7V
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH classification master disabled

16 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2002/95/EC. This includes compliance with the requirements for Deca BDE, as per removal of exemption, implementation date 01-Jul-08
- EU REACH, Regulation (EC) No 1907/2006:
 - List of substances subject to authorisation (Annex XIV)
 - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
 - Substances identified on candidate list as Substances of Very High Concern (SVHC), 53 substances as per update published 20 June 2011.
- EU Commission Decision 2009/251/EC:
 - Products containing dimethylfumarate (DMF) are not placed or made available on the market.
- EU Packaging and Packaging Waste, Directive 94/62/EC
- Montreal Protocol on substances that deplete the ozone layer

Additionally, Table 16.1 shows that CSR Green semiconductor products are free from bromine, chlorine or antimony trioxide and other hazardous chemicals.

| Material | Maximum Allowable Amount |
|---|------------------------------------|
| Cadmium (Cd) | 100ppm |
| Lead (Pb) | 1000ppm (solder), 100ppm (plastic) |
| Mercury (Hg) | 1000ppm |
| Hexavalent-Chromium (Cr VI) | 1000ppm |
| Polybrominated biphenyls (PBB) | 1000ppm |
| Polybrominated diphenyl ethers (PBDE) | 1000ppm |
| Bromine, Chlorine | 900ppm, <1500ppm combined |
| Antimony Trioxide (Sb ₂ O ₃) | 900ppm |
| Benzene | 1000ppm |
| Beryllium and compounds (other than Beryllium Oxide (BeO) | 1000ppm |
| Halogenated Diphenyl Methanes (Monomethyltetrachloro Diphenyl Methane (CAS# 76253-60-6), Monomethyl dichloro Diphenyl Methane (CAS# 81161-70-8), Monomethyl dibromo Diphenyl Methane (CAS# 99788-47-8) | 1000ppm |
| Red phosphorous | 1000ppm |
| 1,1,1-trichloroethane | Banned |

| Material | Maximum Allowable Amount |
|---|--|
| Aliphatic CHCs (chlorohydrocarbons) | Banned |
| Benzotriazole (2-3',5'-Di-tert-butyl-2'-hydroxyphenyl) | Banned |
| Beryllium Oxide | Banned |
| Chlorinated paraffin (including short chain chlorinated paraffins – carbon chain length 10-13 and medium chain chlorinated paraffins – carbon chain length 14-17) | Banned |
| Formaldehyde (Banned in wooden, adhesive and plastic products) | Banned as described |
| Hydrofluorocarbon (HFC) | Banned |
| NPs (nonylphenols) and NPEs (nonylphenol ethoxylates) (Banned in textile, leather, metal, pulp and paper parts) | Banned as described |
| Organic tin compounds | Banned |
| Perfluorocarbon (PFC) | Banned |
| Polychlorinated naphthalenes (PCN) | Banned |
| Polychlorinated terphenyls (PCT) | Banned |
| Polychlorinated biphenyls (PCB) | Banned |
| Polyvinyl Chloride (PVC) | Banned |
| Sulfur hexafluoride | Banned |
| Tetrachloromethane (CAS# 56-23-5) | Banned |
| Asbestos | Banned as intentionally introduced |
| Phthalates | Banned as intentionally introduced |
| Radioactive substances | Banned as intentionally introduced: reportable |
| Tributyl tin (TBT) / Triphenyl tin (TPT) / Tributyl Tin Oxide (TBTO) Dibutyl Tin (DBT) and Dioctyl Tin Compounds (DOT) | Banned as intentionally introduced |

Table 16.1: Chemical Limits for Green Semiconductor Products

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

CSR has defined this Green standard based on current regulatory and customer requirements. For more information contact product.compliance@csr.com.

17 Software

CSR8645 BGA:

- Includes integrated Bluetooth v4.0 specification qualified HCI stack firmware
- Includes integrated CSR8645 Stereo ROM Solution with aptX, with 6th generation 2-mic CVC audio enhancements and a configurable EQ
- Can be shipped with CSR's CSR8645 stereo ROM solution with aptX development kit for CSR8645 BGA, order code DK-8645-10064-1A

The CSR8645 BGA software architecture enables Bluetooth processing and the application program to run on the internal RISC MCU, and the audio enhancements on the Kalimba DSP.

17.1 CSR8645 Stereo ROM Solution with aptX

The CSR8645 stereo ROM solution with aptX software supports:

- 6th generation 2-mic CVC audio enhancements
- WNR
- PLC / BEC
- mSBC wideband speech codec
- A2DP v1.2
- HFP v1.6 and HSP v1.2
- SCMS-T
- Bluetooth v4.0 specification is supported in the ROM software
- Secure simple pairing
- Proximity pairing (headset-initiated pairing) for greatly simplifying the out-of-box pairing process, for more information see Section 17.1.8
- For connection to more than 1 mobile phone, advanced Multipoint is supported. This enables a user to take calls from a work and personal phone or a work phone and a VoIP dongle for Skype users. This has minimal impact on power consumption and is easy to configure.
- Most of the CSR8645 stereo ROM solution with aptX ROM software features are configured on the CSR8645 BGA using the Headset Configurator tool. The tool reads and writes headset configurations directly to the EEPROM, serial flash or alternatively to a PSR file. Configurable headset features include:
 - Bluetooth v4.0 specification features
 - Reconnection policies, e.g. reconnect on power-on
 - Audio features, including default volumes
 - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for last number redial
 - LED indications for states, e.g. headset connected, and events, e.g. power on
 - Indication tones for events and ringtones
 - HFP v1.6 supported features
 - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
 - Advanced Multipoint settings
- Configurable 5-band EQ for music playback (rock, pop, classical, jazz, dance etc)
- aptX, AAC, SBC, MP3 and Faststream decoder
- Stereo widening (S3D)
- Volume Boost
- USB audio mode for streaming high-quality music from a PC whilst charging, enables the headset to:
 - Playback high-quality stereo music, e.g. iTunes
 - Use bidirectional audio in conversation mode, e.g. for Skype

- Wired audio mode for pendant-style headsets supports music playback using a line-in jack. Enables non Bluetooth operation in low battery modes or when using the headset in an airplane-mode.
- Support for smartphone applications (apps)
- The CSR8645 stereo ROM solution with aptX has undergone extensive interoperability testing to ensure it works with the majority of phones on the market

17.1.1 Advanced Multipoint Support

Advanced Multipoint enables the connection of 2 devices to a CSR8645 BGA headset at the same time, examples include:

- 2 phones connected to a CSR8645 BGA headset
- Phone and a VoIP dongle connected to a CSR8645 BGA headset
- Phone and tablet

The CSR8645 stereo ROM solution with aptX:

- Supports up to 2 simultaneous connections (either HFP or HSP)
- Enables multiple-call handling from both devices at the same time
- Treats all headset buttons:
 - During a call from one device, as if there is 1 device connected
 - During multiple calls (1 on each device), as if there is a single AG with multiple calls in progress (three-way calling)
 - During multiple calls (more than 1 on each device), as if there are multiple calls on a single device enabling the user to switch between the active and held calls

17.1.2 A2DP Multipoint Support

A2DP Multipoint support enables the connection of 2 A2DP source devices to CSR8645 BGA at the same time, examples include:

- 2 A2DP-capable phones connected to a CSR8645 BGA headset
- A2DP-capable phone and an A2DP-only source device, e.g. a PC or an iPod touch

The CSR8645 stereo ROM solution with aptX enables:

- Music streaming from either of the connected A2DP source devices where the music player is controlled on the source device
- Advanced HFP Multipoint functions to interrupt music streaming for calls, and resume music streaming on the completion of the calls
- AVRCP v1.4 connections to both connected devices, enabling the headset to remotely control the primary device, i.e. the device currently streaming audio

17.1.3 Wired Audio Mode

CSR8645 BGA supports a wired audio mode for playing music over a wired connection. This enables the headset to operate when the battery is too low for Bluetooth operation or in environments where the use of wireless technologies is not permitted, e.g. airplane-mode.

The CSR8645 stereo ROM solution with aptX automatically routes the wired audio input to the headphone output when CSR8645 BGA is not powered.

If CSR8645 BGA is powered, the audio path is routed through CSR8645 BGA, including via the DSP, this enables the headset to:

- Mix audio sources, e.g. tones and programmable audio prompts
- Control the volume of the audio, i.e. volume up and volume down
- Utilise the 5 band EQ

The wired audio mode can be used in conjunction with the USB audio mode, see Section 17.1.4. USB audio has priority if attached and is routed to the headset speaker if CSR8645 BGA is powered.

In wired audio mode, if required, the headset is still available for Bluetooth audio. This enables seamless transition from wired audio mode to Bluetooth audio mode and back again. This transition is configurable to occur automatically as the battery voltage of the headset reduces to a point at which Bluetooth audio is no longer possible.

The additional development board CNS11010 enables support for the wired input mode and is available as part of the development kit.

17.1.4 USB Modes Including USB Audio Mode

CSR8645 BGA supports a variety of USB modes which enables the USB interface to extend the functionality of a CSR8645 BGA based stereo headset.

CSR8645 BGA supports:

- USB charger enumeration
- USB soundcard enumeration (USB audio mode)
- USB mass storage enumeration

USB audio mode enables the headset to enumerate as a soundcard while charging from a USB master device, e.g. a PC. In this mode, the headset enumerates as either a stereo music soundcard (for high quality music playback) or a bidirectional voice quality soundcard. This enables the headset for either listening to music streaming from the USB host device or for voice applications, e.g. Skype.

The USB audio mode operates at the same time as the wired audio mode and the USB audio interrupts the wired audio mode if USB audio is attached. This enables a headset to have both wired audio and USB modes connected at the same time.

In USB audio mode, if required, the headset is still available for Bluetooth audio.

17.1.5 Smartphone Applications (Apps)

CSR8645 BGA includes CSR's proprietary mechanism for communicating with smartphone apps, it enables full UI control of the headset from within the application running on a smartphone, e.g. Google Android OS-based handset. For more information on this feature contact CSR.

17.1.6 Programmable Audio Prompts

CSR8645 BGA enables a user to configure and load pre-programmed audio prompts from:

- An external EEPROM, in this implementation the prompts are stored in the same EEPROM as the PS Keys, see Figure 17.2. A larger EEPROM is necessary for programmable audio prompts. This implementation supports EEPROMs up to 512Mb. An EEPROM of 512Mb enables approximately 15 seconds of audio storage.
- An external SPI flash, in this implementation the prompts are stored in the same SPI flash as the PS Keys, see Figure 17.1.

The programmable audio prompts provide a mechanism for higher-quality audio indications to replace standard tone indications. A programmable audio prompt is assigned to any user event in place of a standard tone.

Programmable audio prompts contain either voice prompts to indicate that events have occurred or provide user-defined higher quality ring tones/indications, e.g. custom power on/off tones.

The Headset Configurator tool can generate the content for the programmable audio prompts from standard WAV audio files. The tool also enables the user to configure which prompts are assigned to which user events.

Section 6.5 describes the SPI flash interface and Section 7.4 describes the I²C interface to an external EEPROM.

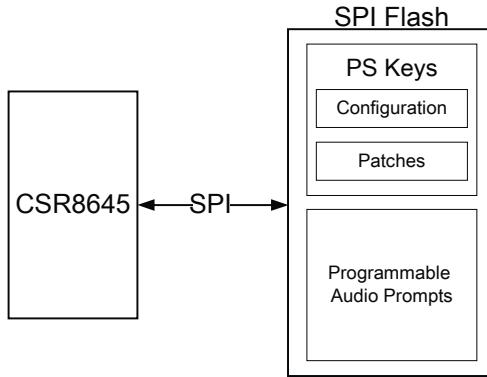


Figure 17.1: Programmable Audio Prompts in External SPI Flash

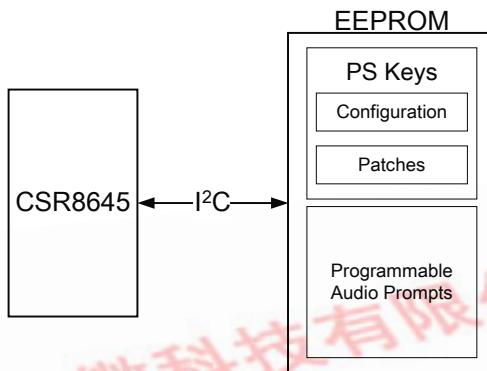


Figure 17.2: Programmable Audio Prompts in External I²C EEPROM

Note:

When using the SPI flash interface for programmable audio prompts, an EEPROM device is not required in the CSR8645 stereo ROM solution with aptX.

17.1.7 CSR's Intelligent Power Management

IPM extends the available talk time of a CSR8645 BGA-based headset, by automatically reducing the audio processing performed by CVC at a series of low battery capacity thresholds.

Configurable IPM features include:

- IPM enable/disable
- The battery capacity that engages IPM
- A user-action to enable or disable the IPM

If engaged, CVC processing reduces automatically on reaching the preset battery capacity. Once the audio is terminated, the DSP shuts down to achieve maximum power savings before the next call.

IPM resets when recharging the headset. The talk time extension depends on:

- The battery size
- The battery condition
- The threshold capacity configured for the IPM to engage

17.1.8 Proximity Pairing

Proximity pairing is headset-initiated pairing and it simplifies the out-of-box pairing process. Proximity pairing enables the headset to find the closest discoverable phone. The headset then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus to pair with the new headset.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the headset pairing is with a PIN code
- For a Bluetooth v2.1 (or above) phone the headset pairing is without a PIN code

Proximity pairing is based on finding and pairing with the closest phone. To do this, the headset finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and it is defined as the closest device. The headset then attempts to pair with and connect to this device.

Proximity pairing is configurable using the Headset Configurator tool available from www.csrsupport.com.

17.1.9 Proximity Connection

Proximity connection is an extension to proximity pairing, see Section 17.1.8. It enables the headset-user to take advantage of the proximity of devices each time the headset powers up and not just during a first time pairing event.

Proximity connection enables a user with multiple handsets to easily connect to the closest discoverable phone by comparing the proximity of devices to the headset at power-on to the list of previously paired devices.

Proximity connection speeds up the headset connection process. It requires the headset to initiate a SLC connection to the nearest device first and combines this with the headset's storage of the last 8 paired/connected devices. Using proximity connection means functions like *power on into an incoming call* operate equally well for the most recently paired or connected device, as well as the least recently paired or connected device.

17.2 6th Generation 2-mic CVC Audio Enhancements

Important Note:

It is important to follow the industrial design considerations in *CVC Two Microphone Headset Design Guidelines* when designing headsets using 2-mic CVC.

2-mic CVC full-duplex voice processing software is a fully integrated and highly optimised set of DSP algorithms developed to ensure easy design and build of echo and noise-cancelling headset products.

CVC enables greater acoustic design flexibility by incorporating software to compensate for cost-optimised microphone-to-speaker coupling and placement. CVC-enabled headsets operate in a wide variety of acoustic environments. Sophisticated noise suppression technology reduces the impact of noise in the transmission channel. Using intelligent volume control and intelligibility improvements, the receive channel is also enhanced based on the acoustic noise in the listener's environment.

The 6th generation CVC provides 3 new major features:

- A high performance Wind Noise Reduction module provides significant reduction of both front and side wind noise. This uses a very low-power algorithm which automatically cuts in only on the detection of wind noise.
- A 16kHz sample rate for full compliance across the suite of DSP algorithms
- Frequency enhanced speech intelligibility

2-mic CVC includes a tuning tool enabling the developer to easily adapt CVC with different audio configurations and tuning parameters. The tool provides real-time system statistics with immediate feedback enabling designers to quickly investigate the effect of changes.

Figure 17.3 shows the functional block diagram of CSR's proprietary 2-mic CVC DSP solution for a dual-microphone headset product.

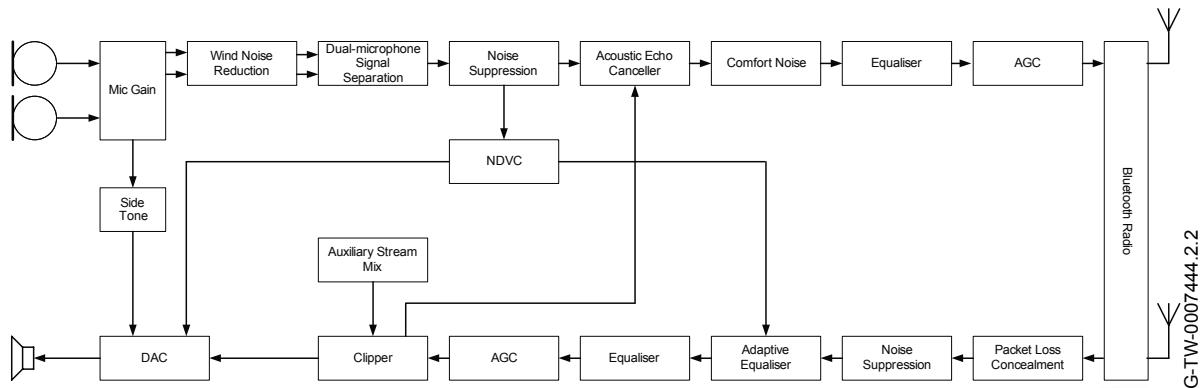


Figure 17.3: 2-mic CVC Block Diagram

Section 17.2.3 to Section 17.2.13 describe the audio processing functions provided within CVC.

17.2.1 Wind Noise Reduction

The wind noise algorithm achieves excellent wind noise reduction with very low power overhead, which has a negligible impact on battery life. The wind noise capability operates in the noise suppression block in the transmit path and dynamically detects and engages when wind noise is present. SNR improvements depend on wind direction, speech and microphone placement. Improvements of up to 32dB are achievable using the DSP module.

CVC wind noise performance is further improved by suitable mechanical baffling of the microphone which is optimised during the tuning process.

17.2.2 Dual-microphone Signal Separation

The dual-microphone signal separation is the major dynamic noise suppression block in 2-mic CVC. It separates the speech from the competing noises. It achieves this by first applying a pre-stage algorithm using a blind source separation processing technique. Blind source separation is a rules based filter which uses the 2 microphones' spatial information, direction of arrival and power ratios assumptions etc.

Blind source separation results in speech (S1) and noise (S2) dominant outputs. These outputs are then processed by a post stage adaptive noise canceller filter to further reduce the environmental noise, resulting in a single-channel noise suppressed output. Depending on the acoustic arrangement of the microphone and the noise type, the dual-microphone signal separation block provides up to 22dB SNR of dynamic noise suppression.

17.2.3 Noise Suppression

The noise suppression block is implemented in both signal paths. It is independent and is individually tuned. Noise suppression is a sub-band stationary / quasi-stationary noise suppression algorithm that uses the temporal characteristics of speech and noise to remove the noise from the composite signal while maximising speech quality. The current implementation can improve the SNR by up to 20dB.

17.2.4 Acoustic Echo Cancellation

The AEC includes:

- A referenced sub-band adaptive linear filter that models the acoustic path from the receive reference point to the microphone input
- A Non-Linear Echo Reduction feature to address severe and distorted echo in speakerphones and car-kits. CVC measures the amount of residual echo after the primary AEC adaptive filter. If the residual echo exceeds a threshold, the NLER function will insert attenuation during far end speech activity, significantly reducing the echo.

17.2.5 Comfort Noise Generator

The CNG:

- Creates a spectrally and temporally consistent noise floor for the far-end listener.
- Adaptively inserts noise modelled from the noise present at the microphone into gaps introduced when the non-linear processing of the AEC applies attenuation. The noise level applied is user-controllable.

17.2.6 Equalisation

The equalisation filters:

- Have independent equalisation modules provided in the send and receive signal paths:
 - Each module comprises of 5 bands of equalisation using cascaded 2nd order IIR filters
- Are fully configurable using a graphical tuning tool
- Provide static compensation for the frequency response of transducers in the system

17.2.7 Automatic Gain Control

The AGC block attempts to:

- Normalise the amplitude of the incoming audio signal to a desired range to increase perceived loudness
- Reduce distortion due to clipping
- Reduce amplitude variance observed from different users, phones and networks

Maintaining a consistent long-term loudness for the speech ensures it is more easily heard by the listener and it also provides the subsequent processing block a larger amplitude signal to process. The behaviour of the AGC differs from a dynamic range audio compressor. The convergence time for the AGC is much slower to reduce the non-linear distortion.

17.2.8 Packet Loss Concealment

Bit errors and packet loss can occur in the Bluetooth transmission due to a variety of reasons, e.g. Wi-Fi interference or RF signal degradation due to distance or physical objects. As a result of these errors, the user hears glitches referred to as *pops* and *clicks* in the audio stream. The PLC block improves the receive path audio quality in the presence of bit and packet errors within the Bluetooth link by using a variety of techniques such as pitch-based waveform substitution.

The PLC significantly improves dealing with bit errors, using the BFI output from the firmware. The DSP calculates an average BER and selectively applies the PLC to the incoming data. This optimises audio quality for a variety of bit errors and packet loss conditions. The PLC is enabled in all modes.

17.2.9 Adaptive Equalisation

The adaptive equalisation block improves the intelligibility of the receive path voice signal in the presence of near-end noise by altering the spectral shape of the receive path signal while maintaining the overall power level. The adaptive equaliser can also compensate for variations in voice transmission channels.

17.2.10 Auxiliary Stream Mix

The auxiliary stream mixer enables the system to seamlessly mix audio signals such as tones, beeps and voice prompts with the incoming SCO stream. This avoids any interruption to the SCO stream and as a result prevents any speech from being lost.

17.2.11 Clipper

The clipper block intentionally limits the amplitude of the receive signal prior to the reference input of the AEC to more accurately model the behaviour of the post reference input blocks such as the DAC, power amplifier and the loudspeaker. This processing block can significantly improve the echo performance in cost-optimised loudspeakers.

17.2.12 Noise Dependent Volume Control

The NDVC block improves the intelligibility of the receive path signal by increasing the analogue DAC gain value based on the send noise estimate from the send path noise suppression block. As the send noise estimate increases, the NDVC algorithm increases the analogue DAC gain value. The NDVC uses hysteresis to minimise the artefacts generated by rapidly adjusting the DAC gain due to the fluctuation in the environmental noise.

17.2.13 Fixed Gains

There are fixed gain controls at all inputs and outputs to the system so that levels are set according to hardware constraints and industry standards.

17.2.14 Frequency Enhanced Speech Intelligibility

Frequency enhanced speech intelligibility on the CSR8645 BGA works with the adaptive equalisation module, see Section 17.2.9, and the NDVC module, see Section 17.2.12, to enhance intelligibility in the presence of noise. This combination of functions creates higher frequency information, which in the presence of noise, makes it much easier for the listener to differentiate between consonant pairs, therefore improving intelligibility. This also reduces listener fatigue as it requires less concentration effort from the user. This can lead to improved dual-tasking performance.

17.3 Music Enhancements

17.3.1 Audio Decoders

CSR8645 BGA supports:

- aptX decoder
- A wide range of standard decoders:
 - SBC
 - MP3
 - AAC
- Faststream codec:
 - Low-latency
 - No video/lip-sync issues while watching a video or playing games
- Jitter handling and high quality sample rate matching
- Low power consumption

17.3.2 aptX Decoder

The aptX audio decoder is available for high-quality stereo audio over Bluetooth. When incorporated in Bluetooth A2DP stereo products, aptX audio coding delivers full *wired* audio quality. The aptX audio codec source material is delivered transparently over the Bluetooth link, whether it is stored uncompressed or in an alternative compression (MP3, AAC, FLAC) format.

Target applications for the aptX decoder include:

- Bluetooth stereo headphones / headsets
- Bluetooth automotive audio
- Bluetooth stereo speakers

Benefits of the aptX decoder include:

- Outstanding Bluetooth Stereo audio quality
- Faithful reproduction of full audio bandwidth
- Minimization of 'lip-sync' issues via low-delay audio decoding techniques
- Non-destructive transcoding from other standard coded audio formats
- Low code memory and data memory requirements
- A2DP-compliant negotiation back to the SBC decoder when connecting with legacy audio sources

Key features of the aptX decoder include:

- Multiple audio sample rate support, including $F_s = 44.1$ kHz and $F_s = 48$ kHz
- Conveyance of CD-quality audio (16-bit and $F_s = 44.1$ kHz) over Bluetooth at a data rate of 352 kbps
- Frequency response maintained from 10 Hz to 22 kHz for $F_s = 48$ kHz
- Algorithmic delay less than 1.89 ms for $F_s = 48$ kHz
- Dynamic range for 16-bit audio in excess of 92 dB

17.3.3 Configurable EQ

The configurable equaliser on the CSR8645 BGA:

- Each EQ filter contains up to 5 fully tuneable stages of cascaded 2nd order IIR filters per bank
- Enables compensation for imperfections in loudspeaker performance and frequency adjustments to the received audio to enhance music brightness
- Contains tiering for multiple customer presets, e.g. rock, pop, classical, jazz, dance etc.
- Contains an easy to use GUI, with drag points, see Figure 17.4

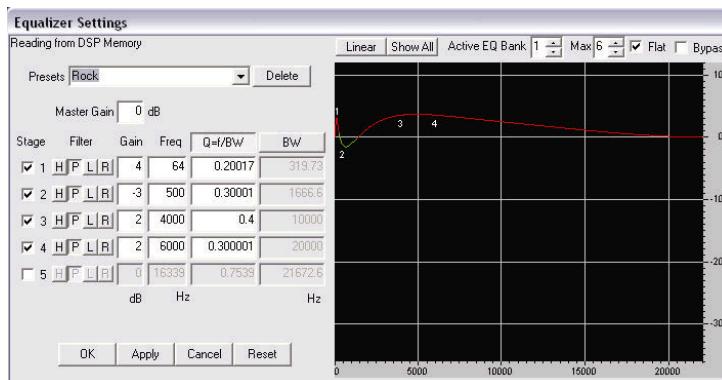


Figure 17.4: Configurable EQ GUI with Drag Points

- Is configurable with up to 6 switchable bank presets. This enables the headset user to select between the EQ bank presets through button presses.

17.3.4 Stereo Widening (S3D)

The stereo widening feature on CSR8645 BGA:

- Simulates loudspeaker listening to provide 3D listening experience
- Is highly optimised at <1MIPS of the Kalimba DSP
- Reduces listener fatigue for headphone listening

17.3.5 Volume Boost

The volume boost feature on the CSR8645 BGA is a dynamic range compander and provides:

- Additional loudness without clipping
- Multi-stage compression and expansion
- Processing modules for dynamic bass boost
- Easy to use GUI, with drag points, see Figure 17.5

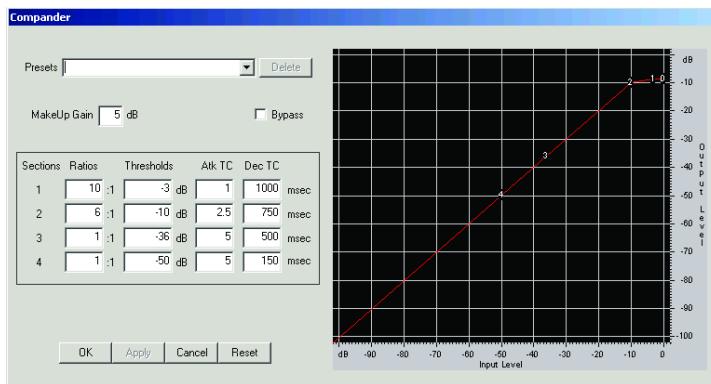


Figure 17.5: Volume Boost GUI with Drag Points

- Louder audio output without distortion

17.4 CSR8645 Stereo ROM Solution with aptX Development Kit

CSR's audio development kit for the CSR8645 BGA, order code DK-8645-10064-1A, includes a CSR8645 stereo ROM solution with aptX demonstrator board and necessary interface adapters and cables are available. In conjunction with the CSR8600 ROM Series Configuration Tool and other supporting utilities the development kit provides the best environment for designing audio solutions with the CSR8645 BGA.

Important Note:

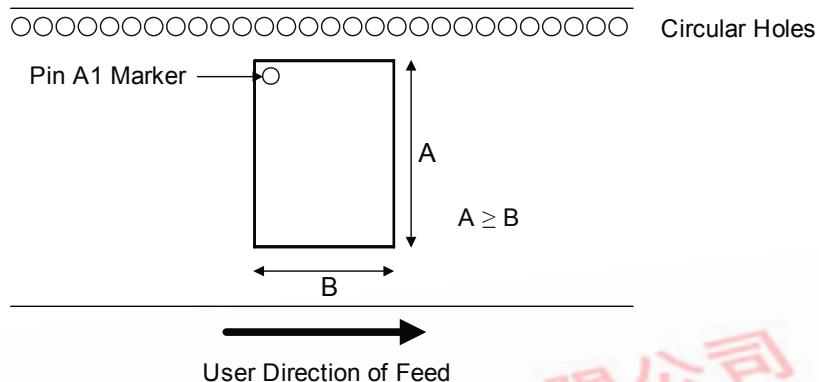
The CSR8645 Stereo ROM Solution with aptX audio development kit is subject to change and updates, for up-to-date information see www.csrsupport.com.

18 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

18.1 Tape Orientation

Figure 18.1 shows the general orientation of the CSR8645 BGA package in the carrier tape.

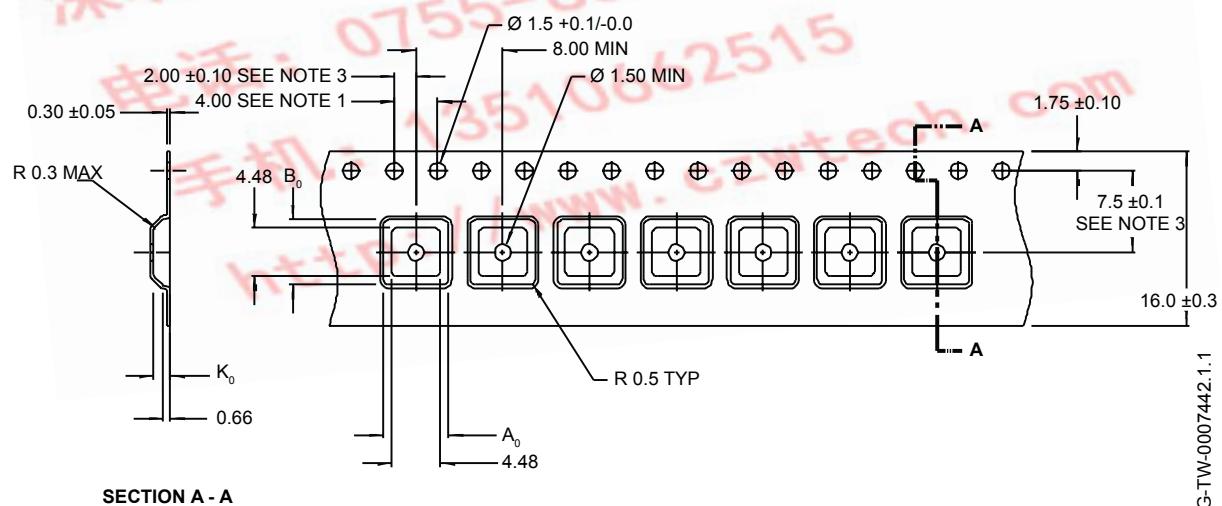


G-TW-0002434.3.2

Figure 18.1: Tape Orientation

18.2 Tape Dimensions

Figure 18.2 shows the dimensions of the tape for the CSR8645 BGA.



G-TW-0007442.1.1

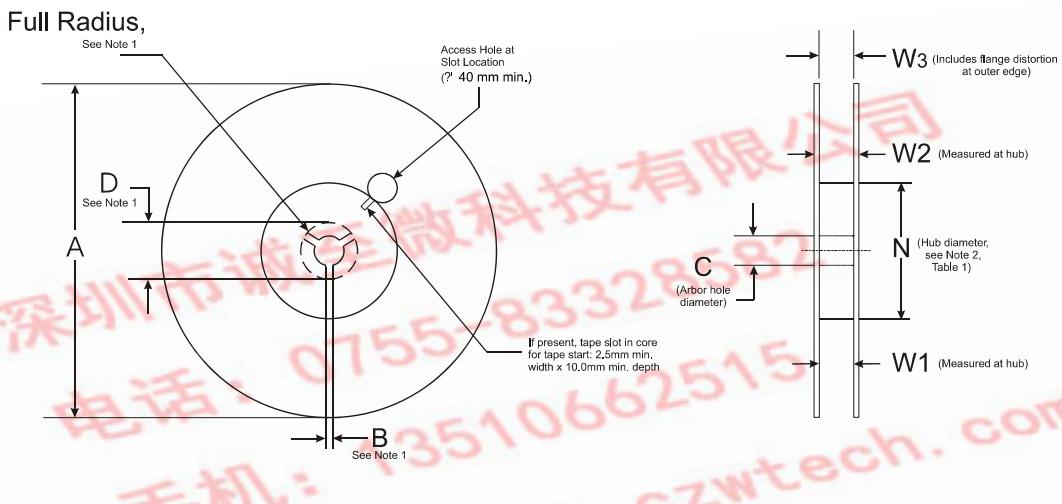
Figure 18.2: Tape Dimensions

| A_0 | B_0 | K_0 | Unit | Notes |
|-------|-------|-------|------|--|
| 6.00 | 6.00 | 1.50 | mm | 1. 10 sprocket hole pitch cumulative tolerance ± 0.2 . 2. Camber in compliance with EIA 481. 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole 4. Tolerances, unless noted, 1PL ± 0.2 , 2PL ± 0.10 5. Material: PS + C |

18.3 Reel Information

Reel dimensions

(All dimensions in millimeters)



GTW40000863.2

Figure 18.3: Reel Dimensions

| Package Type | Tape Width | A Max | B | C | D Min | N Min | W1 | W2 Max | W3 | | Units |
|-----------------------|------------|-------|-----|-----------------|-------|-------|-----------------|--------|------|------|-------|
| | | | | | | | | | Min | Max | |
| 5.5 x 5.5 x 1mm VFBGA | 16 | 332 | 1.5 | 13.0 (0.5/-0.2) | 20.2 | 50 | 16.4 (3.0/-0.2) | 19.1 | 16.4 | 19.1 | mm |

18.4 Moisture Sensitivity Level

CSR8645 BGA is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

19 Document References

| Document | Reference, Date |
|---|---|
| <i>BlueCore Audio API Specification</i> | CS-209064-DD |
| <i>BlueTest User Guide</i> | CS-102736-UG |
| <i>Bluetooth and USB Design Considerations</i> | CS-101412-AN |
| <i>Core Specification of the Bluetooth System</i> | Bluetooth Specification Version 4.0, 17 December 2009 |
| <i>CSR8645 BGA Performance Specification</i> | CS-218184-SP |
| <i>Electrostatic Discharge (ESD) Sensitivity Testing, Machine Model (MM)</i> | JESD22-A115C |
| <i>ESDA/JEDEC Joint Standard For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level</i> | ANSI/ESDA/JEDEC JS-001-201 |
| <i>Field-Induced Charged-Device Model Test Method for Electrostatic- Discharge-Withstand Thresholds of Microelectronic Components</i> | JESD22-C101E |
| <i>IC Packing and Labelling Specification</i> | CS-112584-SP |
| <i>IEC 61000-4-2 Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test</i> | IEC 61000-4-2, Edition 2.0, 2008-12 |
| <i>Kalimba Architecture 3 DSP User Guide</i> | CS-202067-UG |
| <i>Lithium Polymer Battery Charger Calibration and Operation for CSR8670</i> | CS-204572-AN |
| <i>Moisture / Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices</i> | IPC / JEDEC J-STD-020 |
| <i>Optimising BlueCore5-Multimedia ADC Performance Application Note</i> | CS-120059-AN |
| <i>Selection of I²C EEPROMS for Use with BlueCore</i> | bcore-an-008P |
| <i>Typical Solder Reflow Profile for Lead-free Device</i> | CS-116434-AN |
| <i>Universal Serial Bus Specification</i> | v2.0, 27 April 2000 |
| <i>USB Battery Charging Specification</i> | v1.1, 15 April 2009 |

Terms and Definitions

| Term | Definition |
|---------------|--|
| 8DPSK | 8-phase Differential Phase Shift Keying |
| $\pi/4$ DQPSK | $\pi/4$ rotated Differential Quaternary Phase Shift Keying |
| μ -law | Audio companding standard (G.711) |
| A-law | Audio companding standard (G.711) |
| A2DP | Advanced Audio Distribution Profile |
| AAC | Advanced Audio Coding |
| AC | Alternating Current |
| ACL | Asynchronous Connection-oriented |
| ADC | Analogue to Digital Converter |
| AEC | Acoustic Echo Cancellation |
| AEQ | Adaptive Equaliser |
| AFC | Automatic Frequency Control |
| AFH | Adaptive Frequency Hopping |
| AG | Audio Gateway |
| AGC | Automatic Gain Control |
| ALU | Arithmetic Logic Unit |
| AVRCP | Audio/Video Remote Control Profile |
| BCCMD | BlueCore Command |
| BCSP | BlueCore Serial Protocol |
| BEC | Bit Error Concealment |
| BER | Bit Error Rate |
| BFI | Bad Frame Indicator |
| BIST | Built-In Self-Test |
| BlueCore® | Group term for CSR's range of Bluetooth wireless technology ICs |
| Bluetooth® | Set of technologies providing audio and data transfer over short-range radio connections |
| BMC | Burst Mode Controller |
| CNG | Comfort Noise Generation |
| codec | Coder decoder |

| Term | Definition |
|--------|---|
| CRC | Cyclic Redundancy Check |
| CSR | Cambridge Silicon Radio |
| CTS | Clear to Send |
| CVC | Clear Voice Capture |
| CVSD | Continuous Variable Slope Delta Modulation |
| DAC | Digital to Analogue Converter |
| DC | Direct Current |
| DDS | Direct Digital Synthesis |
| DMA | Direct Memory Access |
| DNL | Differential Non Linearity (ADC accuracy parameter) |
| DSP | Digital Signal Processor (or Processing) |
| DUT | Device Under Test |
| e.g. | <i>exempli gratia</i> , for example |
| EDR | Enhanced Data Rate |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EIA | Electronic Industries Alliance |
| EMC | Electromagnetic Compatibility |
| EQ | Equaliser |
| eSCO | Extended SCO |
| ESD | Electrostatic Discharge |
| ESR | Equivalent Series Resistance |
| etc | <i>et cetera</i> , and the rest, and so forth |
| FIR | Finite Impulse Response (filter) |
| FSK | Frequency Shift Keying |
| G.722 | An ITU-T standard wideband speech codec operating at 48, 56 and 64 kbps |
| GCI | General Circuit Interface |
| GSM | Global System for Mobile communications |
| GUI | Graphical User Interface |
| H4DS | H4 Deep Sleep |
| HBM | Human Body Model |

| Term | Definition |
|------------------|--|
| HCI | Host Controller Interface |
| HFP | Hands-Free Profile |
| HSP | HeadSet Profile |
| I ² C | Inter-Integrated Circuit Interface |
| I ² S | Inter-Integrated Circuit Sound |
| i.e. | <i>Id est</i> , that is |
| I/O | Input/Output |
| IC | Integrated Circuit |
| IEEE | Institute of Electronic and Electrical Engineers |
| IF | Intermediate Frequency |
| IIR | Infinite Impulse Response (filter) |
| INL | Integral Non Linearity (ADC accuracy parameter) |
| IPM | Intelligent Power Management |
| IQ | In-Phase and Quadrature |
| ISDN | Integrated Services Digital Network |
| JEDEC | Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association) |
| Kalimba | An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression, and file compression / decompression |
| Kb | Kilobit |
| LC | An inductor (L) and capacitor (C) network |
| LDO | Low (voltage) Drop-Out |
| LED | Light-Emitting Diode |
| LM | Link Manager |
| LNA | Low Noise Amplifier |
| LSB | Least Significant Bit (or Byte) |
| MAC | Multiplier and ACcumulator |
| Mb | Megabit |
| MCU | MicroController Unit |
| MEMS | Micro Electro Mechanical System |
| MIPS | Million Instructions Per Second |

| Term | Definition |
|--------|---|
| MISO | Master In Slave Out |
| MLC | Multilayer Ceramic |
| MMU | Memory Management Unit |
| MP3 | MPEG-1 audio layer 3 |
| mSBC | modified Sub-Band Coding |
| N/A | Not Applicable |
| NDVC | Noise Dependent Volume Control |
| NSMD | Non Solder Mask Defined |
| PA | Power Amplifier |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PCM | Pulse Code Modulation |
| PIN | Personal Identification Number |
| PIO | Parallel Input/Output |
| PIO | Programmable Input/Output, also known as general purpose I/O |
| PLC | Packet Loss Concealment |
| plc | Public Limited Company |
| PS Key | Persistent Store Key |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RC | A Resistor and Capacitor network |
| RF | Radio Frequency |
| RGB | Red Green Blue |
| RISC | Reduced Instruction Set Computer |
| RoHS | Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC) |
| ROM | Read Only Memory |
| RSSI | Received Signal Strength Indication |
| RTS | Request To Send |
| RX | Receive or Receiver |
| SBC | Sub-Band Coding |

| Term | Definition |
|--------|--|
| SCL | Serial Clock Line |
| SCMS | Serial Copy Management System (SCMS-T). A content protection scheme for secure transport and use of compressed digital music |
| SCO | Synchronous Connection-Oriented |
| SDA | Serial Data (line) |
| SIG | (Bluetooth) Special Interest Group |
| SLC | Service Level Connection |
| SMPS | Switch Mode Power Supply |
| SNR | Signal-to-Noise Ratio |
| SPI | Serial Peripheral Interface |
| TBD | To Be Defined |
| THD+N | Total Harmonic Distortion and Noise |
| TX | Transmit or Transmitter |
| UART | Universal Asynchronous Receiver Transmitter |
| UI | User Interface |
| USB | Universal Serial Bus |
| VCO | Voltage Controlled Oscillator |
| VFBGA | Very thin, Fine pitch, Ball Grid Array |
| VM | Virtual Machine |
| VoIP | Voice over Internet Protocol |
| W-CDMA | Wideband Code Division Multiple Access |
| Wi-Fi® | Wireless Fidelity (IEEE 802.11 wireless networking) |
| WNR | Wind Noise Reduction |